

A MICROPROCESSOR CONTROLLED COLOR IMAGE SCANNER

Åke E. Nygren



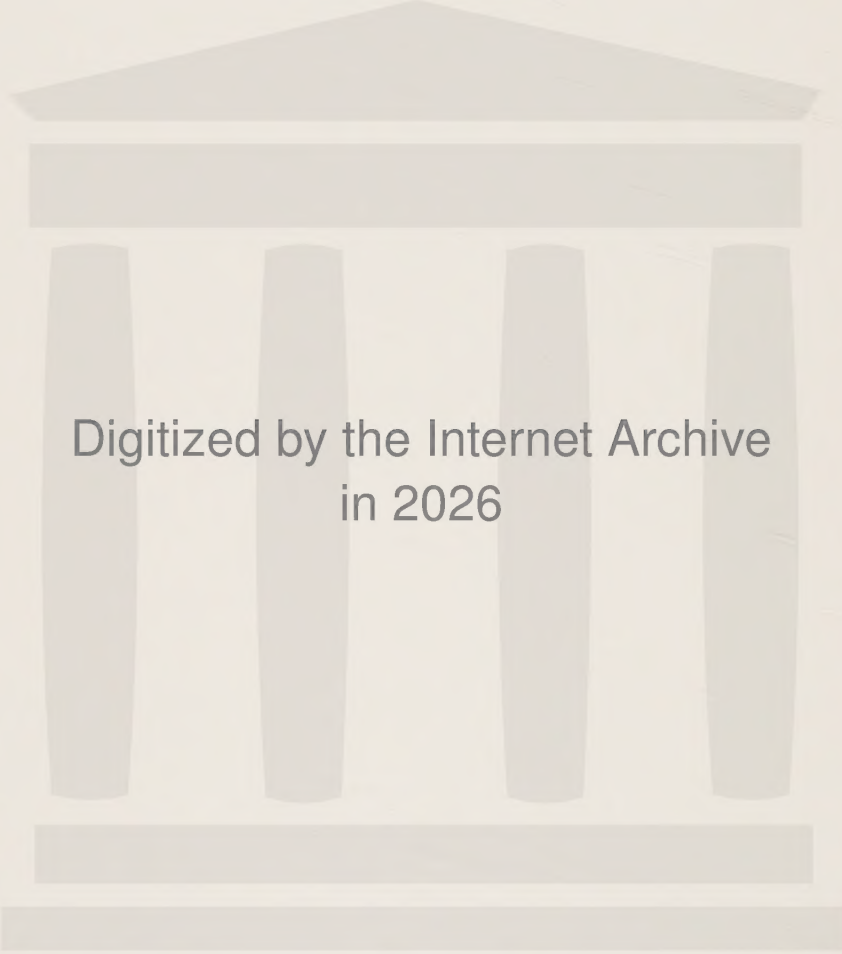
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COLOR IMAGE SCANNER

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ABSTRACT

The development of the electronic circuitry for a color image scanner is described. A microprocessor system has been used as the process controller, which gives the scanner system great flexibility in it's operation. The scanner converts a continuous tone color image into a bilevel color representation, and stores this digital information on a 0.5" standard 9 channel computer magnetic tape. The entire scanner system is controlled through an interrupt system which optimizes the use of the microprocessor by reducing the system overhead. The program controlled transfer of a scan line of image information in the three primary colors (magenta, yellow and cyan) into the processor memory is carried out concurrently with the transfer of the previous scan line from the memory to the magtape station. This latter transfer is controlled by a transparent DMA controller which uses the address and data busses for DMA transfers when the microprocessor is not using them. Hence the microprocessor is not affected by the DMA transfers and can operate at normal speed. This solution makes it possible to handle all tasks in the scanner system with only one microprocessor.

After a general introduction and description of the scanner system, the report centers on the software and hardware implementation of the scanner system.



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1 INTRODUCTION

1.1 Background

During 1970-72 an ink jet color plotter was developed at the department of Electrical Measurements, Lund Institute of Technology (Smeds 1973). The plotter was later improved by Bladh (1982). As shown in Fig. 1-1, the plotter consists of three ink jets with the colors magenta, yellow and cyan, which are mounted on a common carriage that is slowly moved by a screw drive parallel to the surface of the drum rotating with a constant speed. For each revolution of the drum, the carriage carrying the three ink jets is moved sideways 0.2 mm, generating a recording line density of 5 lines/mm.

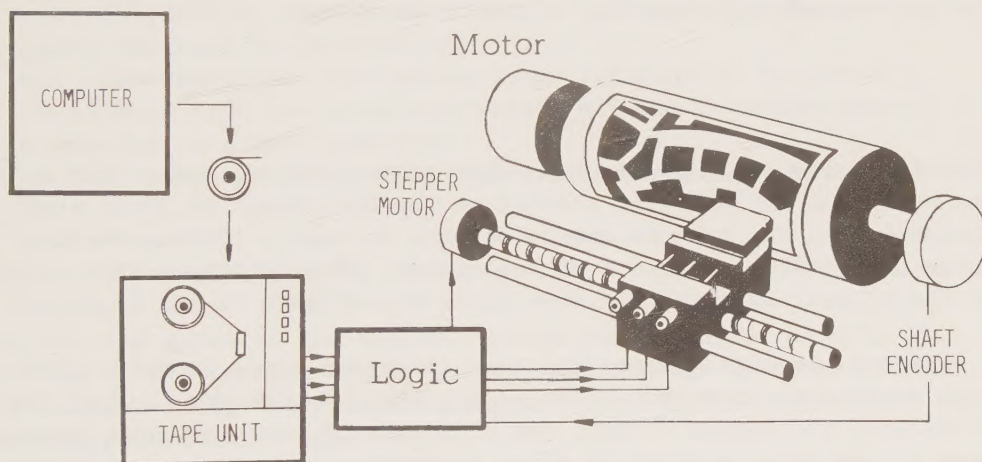


Fig 1-1 Basic units of the color jet plotter. The information to be plotted is computed in a suitable format by the computer and stored on a magnetic tape. This tape is then read by a magnetic tape unit into a buffer memory. The read-in and read-out periods of the memory are governed by control circuits, and the read-out signals are used to modulate the intensity of the three ink jets (magenta, yellow and cyan) mounted on a common carriage in front of the rotating drum carrying the recording paper.

The same resolution is maintained along the recording line through the shaft encoder mounted on the drum axis. The plotter uses continuous ink jets which are on/off modulated by electrical signals in a special electrode system (Hertz and Månsson, 1972). Thus the plotter is a bilevel device and cannot print continuous-tone images. Therefore, a raster method must be used to make this possible.

In 1973 Jern started the development of a graphic color raster software package for image generation on the ink jet plotter (Jern 1978). The software package accepted input data in numerical form, as vectors, polygons, etc., and converted them into raster format, but there was no facility to enter an image directly in raster format.

In several applications a base map or background is necessary to understand the results presented in the output image. As an example, an image showing the sulphur pollution in an area would be impossible to interpret unless a map over the area was added to the input data. Due to the high cost of manually digitized base maps and backgrounds, the plotter was not used to its potential extent.

1.2 Present work

Therefore, the development of a color image scanner, compatible with the color ink jet plotter, started at the Department of Electrical Measurements. The scanner should be able to read a continuous-tone image and convert it into a bilevel image. After plotting, the colors of the bilevel image should show close resemblance to the original.

A prototype of this scanner has been operative since December 1979 and used in some applications (Jern et al. 1981, Nygren and Lindahl 1983). In Nilsson and Nygren (1981A) the principle of the conversion method used in the color scanner is given together with a general description of the scanner. The selection of suitable threshold algorithms, the modifications in hardware and software due to different characteristics between the scanner and the output device, and other vital aspects for good color image rendition in the bilevel image, are given in Nilsson and Nygren (1981B)

To arrive at the results mentioned above a microprocessor controlled scanner was used. This report gives a detailed technical description of the electronic design of the scanner and the associated software necessary to operate it.

2 GENERAL DESCRIPTION OF THE SCANNER

2.1 Design considerations

2.1.1 Scanner - plotter compatibility

Since compatibility with the ink jet plotter was one of the goals of this design, a few technical specifications and limitations were conditional, such as:

image resolution : 5 lines/mm
drum surface size : 672 * 675 mm
detected colors : magenta, yellow and cyan

Other important design goals were:

- a) flexible system design to allow alterations in the continuous-tone to bilevel conversion algorithm. This is especially useful as an evaluation of different conversion algorithms must be carried out.
- b) real time operation. The analog image information is directly transformed into a bilevel equivalent without intermediate processing in a host computer.
- c) low cost compared to commercially available optical scanners.

2.1.2 Possible implementation methods

The major task given to the scanner system can be illustrated by a simplified block diagram, Fig. 2-1. The analog image information is converted into a digital (bilevel) representation. This conversion can be implemented in three ways:

1. a software implementation where the conversion is achieved in software. This method is too slow to fulfill the real time operation goal.
2. a hardware implementation where the conversion is accomplished in hardware. This method cannot fulfill the flexible system design goal.
3. a firmware implementation which is a combination of hardware and software implementation. This method can combine the flexibility of the software implementation with the real time operation facility of the hardware implementation.

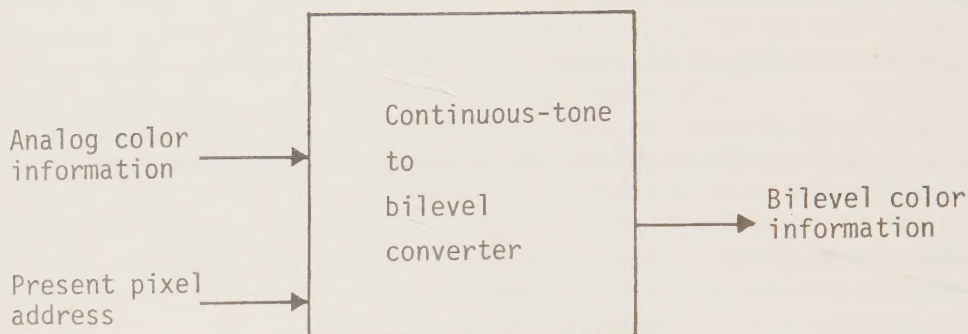


Fig 2-1 Simplified block diagram showing the inputs and output of the scanner system. The converter can be realized using a hardware design, software design or a combination of both.

We chose a firmware implementation in our scanner because of the advantages mentioned above. We also restricted the scanner to non-adaptive pseudo-gray scale algorithms. Our reasons for this restriction are given in Nilsson and Nygren (1981B).

The basic units of the color image scanner are shown in Fig 2-2. Before the system design is described, the flow of data through the scanner from the drum surface to the magnetic tape station (magtape station) and associated timing considerations will be discussed.

2.2 Principle of image information flow through the scanner system

When the illuminated original image is rotating on the drum, the reflected light reaching the scanner head's lens system is color separated pixel by pixel into its three subtractive primary colors, magenta, yellow and cyan. Thereafter each color is detected and amplified separately to suitable levels for the A/D converter. The scanner head and its associated electronics are described in Nilsson (1981) and hence not included in this paper.

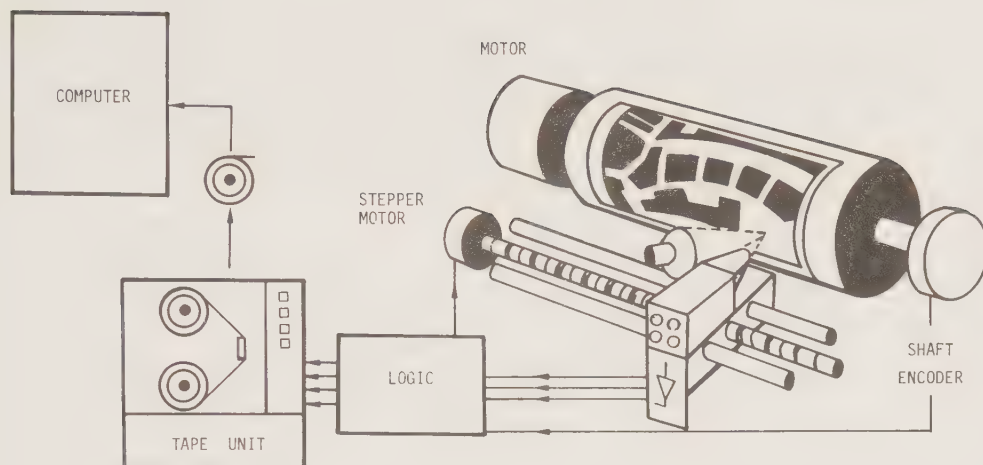


Fig 2-2 Basic unit of the color image scanner. Physically it resembles the plotter in Fig 1-1, but has the recording head replaced by an optical scanner head, and the flow of data reversed. - An original image or map is fastened on the rotating drum and scanned line by line. Each picture element (pixel) is separated into its tricolor contents of magenta, yellow and cyan, and converted into a bilevel representation before it is stored on a magnetic tape.

The principle of image information flow through the scanner system after this analog section is shown in Fig. 2-3. Although the scanner has three identical parallel image channels, in the following only one image channel will be discussed for simplicity.

As shown in the figure, the analog image information is A/D converted into an 8-bit digital value. This value is compared with an 8-bit threshold value in an 8-bit comparator. Depending on the outcome of the comparison either a "1" or a "0" is passed on to the serial to parallel converter. This threshold method is used to generate shades of color by a matrix technique, in which different shades of color can be obtained by on-off modulating the color in e.g. 16 positions of a 4 by 4 matrix (Nilsson and Nygren 1981B). When 8 bits are packed into a byte in the serial to parallel converter, the byte is moved and temporarily stored in a Read Write Memory (RWM).

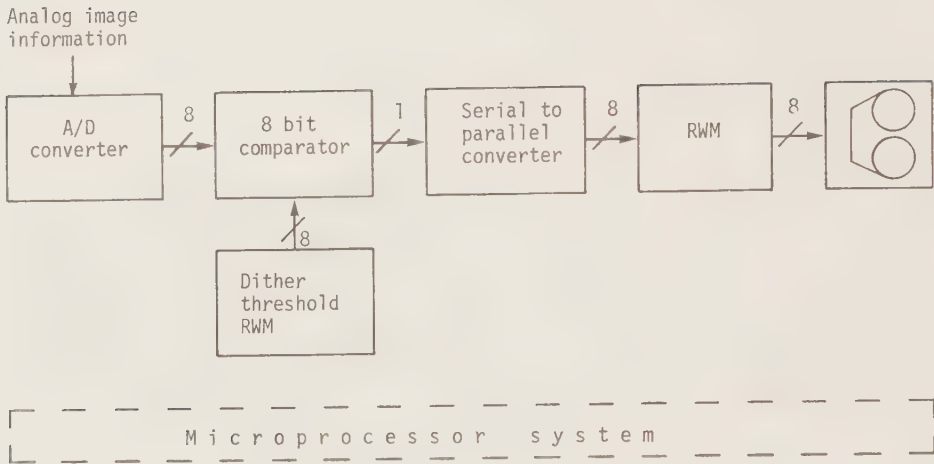


Fig 2-3 Block diagram showing the principals of image information flow through the scanner system. The analog image information is A/D converted pixel by pixel. The resulting 8 bit digital value is compared with a threshold value and the outcome of this comparison, a "1" or a "0", is shifted into the serial to parallel converter (S/P). When 8 bits are shifted into the S/P, the resulting byte is stored in the microprocessor system Read Write Memory (RWM). When the last byte of a scan line is stored in the RWM, the entire scan line is transferred to the magtape station and written on a magnetic tape.

This procedure is repeated until all image information from one scan line is stored in the RWM, whereafter it is transferred to the magtape station and stored on the tape as one record. This sequence is repeated until the entire image is stored on the magtape.

This general description of image information flow shows that the information flow is divided into two separate transfers: one transfer from the A/D converter to the RWM and another transfer from the RWM to the magtape station. Before detailed descriptions of the transfers are given, some knowledge of the time available for the transfers is necessary to understand the selection of transfer methods.

Let us assume that the drum surface is rotating with a maximum surface speed of 5 m/s. At this speed each pixel of 0.2 mm diameter passes the scanner head detectors in 40 μ s. As each pixel gives rise to one bit of information after passing the serial to parallel converter, a new byte is ready to be transferred to the RWM every $8 * 40 = 320$ μ s. Since this information has to be transferred for all three colors, the actual time for the transfer of one byte has to be less than 106 μ s. This can be managed using software running in the microprocessor.

An entire scan line consists of 3072 pixels (bits) = 384 bytes in each color. The time between each transfer from the RWM to the magtape station is therefore somewhat longer than 100 ms. Due to the magtape station and its characteristics the transfer between the RWM and the magtape station must be faster than this. For the present experiments a 37.5 ips, 800 bpi magtape station and a faster 125 ips, 800/1600 bpi magtape station were available. When data is written onto a magnetic tape, the data must be supplied at a constant rate determined by the tape speed and tape density as shown in Table 2-1. If the slow magtape station is used, the transfer of a byte from the RWM to the magtape station must take place every 33.3 μ s, and the entire scan line is then transferred in approximately 80 ms including start and stop time for the magtape. Since this is less than the 100 ms mentioned above, even the slower magtape station available to us could be used here. However, this high transfer speed cannot be achieved by software control. Therefore a special DMA controller has been designed for this task (Nygren et al. 1980).

tape speed <ips>	packing density <bpi>	transfer rate <kbytes/s>
37.5	800	30
125	1600	100
125	1600	200

Table 2-1 Transfer rate as a function of magtape station speed and packing density of the tape.

2.3 Transfer from the A/D converter to the RWM

A more detailed block diagram of the circuitry used in the image information transfer from the A/D converter to the RWM is given in Fig. 2-4. The 8-bit A/D converter (Micro Networks MN5150) uses the successive approximation conversion method, and a complete conversion takes approximately 8 clock cycles, which is equal to 4 μ s in the scanner system. The start of each conversion is controlled by the bit strobe signal, BSTB2, from the shaft encoder circuit mounted on the drum axis. The signal BSTB2, called BSYNK in Nilsson and Nygren (1981A), starts a new conversion every 0.1 mm movement of the drum surface. The digital output of the A/D converter is continuously compared to the threshold value from the Dither threshold RWM and the resulting bit of the comparison is shifted into a serial to parallel converter (S/P1) when the comparator output value is valid. For each A/D conversion a new bit is shifted into S/P1, resulting in two bits of information per 0.2 mm pixel. To reduce this information to one bit per 0.2 mm pixel a digital lowpass filter is used.

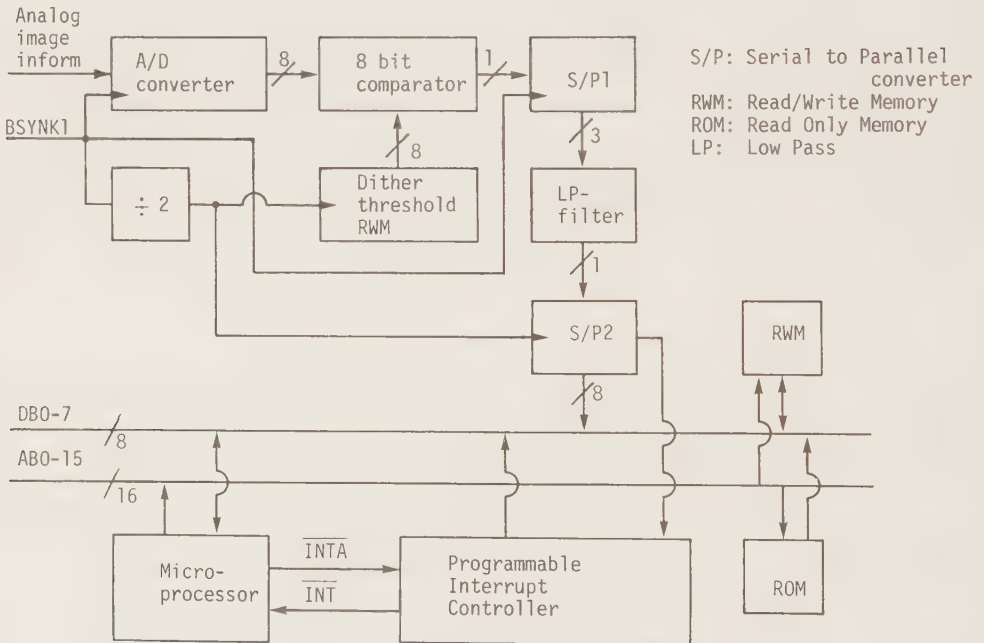


Fig 2-4 Block diagram showing the hardware used for the transfer of image information from the A/D converter to the RWM. For clarity the address bus connections to the devices, such as the programmable interrupt controller, are not shown.

The circuit compares 3 consecutive bits from S/P1 and output the logic level which is in majority. Since the clock frequency of serial to parallel converter, S/P2, is half of the clock frequency of S/P1, the number of bits per 0.2 mm is reduced to one. S/P2 is packing the pixel information bits into bytes. When a byte is packed, it is transferred to the RWM.

Since the RWM is a part of the microprocessor system, this latter transfer involves that system. To this end the byte is first transferred into a register in the microprocessor. Then an address is selected in the RWM, and the byte is moved to this RWM address and stored there. This sequence is repeated for the other two colors, and the entire transfer takes less than 175 μ s. As there are 320 μ s available for these transfers, a simple program controlled transfer method is sufficient.

To be able to make the transfers, the microprocessor must know when the bytes are packed. A commonly used method in cases like this is called polling. A program running in the microprocessor constantly checks a hardware register to see when the bytes are packed. The program will use all processing time available aside from the actual transfer time. This performance degrading method cannot be used in the scanner as the processor must be used to control and monitor several other activities. Instead a Programmable Interrupt Controller (PIC) is added. The PIC replaces the polling program, and the microprocessor can use its processing time for other tasks. The PIC has its interrupt request lines connected to events like the packing of bytes. When the bytes are packed, the PIC receives an interrupt request, and it directly requests the microprocessor to discontinue processing the current program and start executing the service routine for this particular interrupt. In Fig. 2-4 the signal IR2 informs the PIC that the bytes are packed and ready to be transferred. If the interrupt system in the microprocessor is enabled, the microprocessor will acknowledge the request after the present instruction is completed. The PIC gives the start address of the interrupt service routine to the microprocessor, and the microprocessor starts executing it. When the service routine is completed, the processor resumes processing the previous program. A more detailed description of the PIC and its functions will be given in chapter 3.4.1 and 4.2.3.

2.4 Transfer from the RWM to the magtape station

A more detailed block diagram of the circuitry used to transfer the image information from the RWM to the magtape station is given in Fig. 2-5. When all bytes of a scan line are transferred into the RWM, the microprocessor must transfer this scan line from the RWM to the magtape station. Since the time available for this transfer is quite short (33.3 μ s/byte, c.f. chapter 2.2) it cannot be carried out under program control.

This is especially true since the transfer from the A/D converter to the RWM is being executed concurrently and utilizing approx. 50% of the available processing time. A solution to this problem is to use Direct Memory Access (DMA) transfers. DMA transfer is a technique where a memory start address and the number of consecutive bytes to transfer to or from the memory are given to a DMA controller. The controller thereafter moves data without involving the microprocessor.

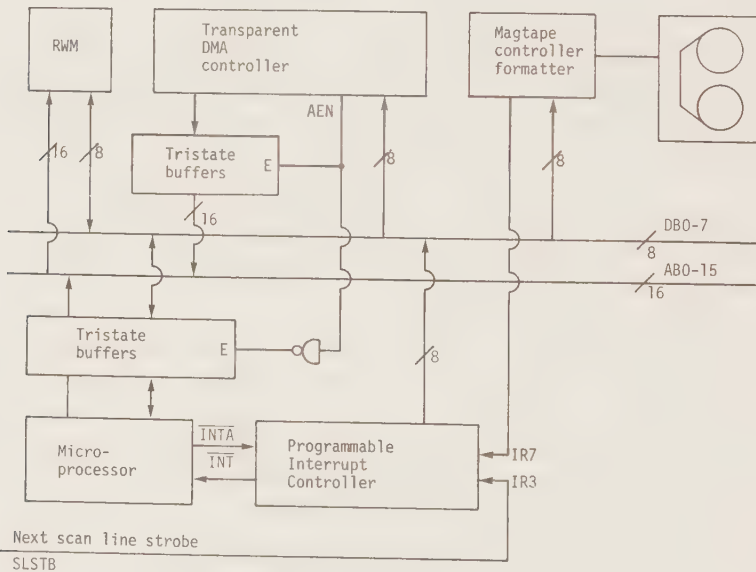


Fig 2-5 Block diagram showing the hardware used for transfers of image information from the microprocessor system RWM to the magtape station. For clarity the address bus connections to the devices, such as the programmable interrupt controller, are not shown.

In the scanner, the DMA controller moves a byte from the RWM to the magtape station, using the normal address and data busses. Thereafter it increments its memory address pointer, decrements the number of consecutive bytes to transfer counter and waits for a signal from the magtape formatter to transfer the next byte. This transfer method is fast and commercially available DMA controllers, such as INTEL 8257, can handle the 200 kHz transfer rate necessary to interface the scanner system with an 125 ips, 1600 bpi magtape station. However, there is one major drawback with these DMA controllers. The microprocessor's normal program execution is suspended during the DMA transfers. At the 200 kHz transfer rate of the 8257 DMA controller, the 8080A microprocessor used in the scanner system is performing at less than half its normal execution speed. The program controlled transfer from the A/D converter to the RWM will then require more time than is available and data loss will occur in these transfers. To avoid this and to allow for future improvements, such as higher optical resolution and higher drum surface speed, a special DMA controller was designed (Nygren et al. 1980). This controller will be described in the following chapter.

2.5 Transparent DMA controller

This DMA controller is based on the fact that the 8080A microprocessor is not using the address and data busses at all times during the execution of an instruction. Thus there is time available during which these busses can be used for DMA transfers.

The 8080A instructions are divided into machine cycles and states according to Fig. 2-6. All instructions consist of at least one machine cycle with three states, T1-T3. The processor only uses the address and data bus during two of them, T2 and T3, independent of whether the machine cycle contains 3, 4 or 5 states. The remaining states are free to use for DMA transfers.

In the worst case when all instructions executed contain 3 states and the execution time of each state is 500 ns. Then a DMA transfer can occur in every 1.5 μ s, and the peak transfer rate will exceed 600 kbytes/s without affecting the microprocessor's normal program execution.

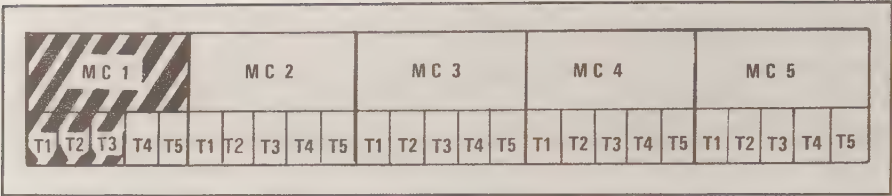


Fig 2-6 Each of the 8080A processor instructions is divided in up to 5 machine cycles depending on the complexity of the instruction. The machine cycle itself is divided into 3-5 states, each 500 ns long. All instructions consists of at least 1 machine cycle with 3 states, T1 through T3. - During states T2 and T3, the processor utilizes the address and data busses, while the busses are free during the remaining states for other tasks.

The DMA transfer of a scan line is started by the interrupt request line IR3 from the "next scan line" detector in the shaft encoder (c.f. Fig 2-5). The processor sets the RWM address counter in the DMA controller and issues a start instruction. The processor thereafter resumes moving data from the S/P2 to another area in the RWM. Simultaneously the DMA controller transfers the first byte. The following transfers of bytes to the magtape station are controlled by the magtape formatter, which requests a new byte immediately after the previous byte has been written onto the magtape. When the DMA controller has transferred the last byte, it signals the magtape formatter which stops the tape movement and thereafter generates a DMA transfer completed interrupt request on the interrupt request line IR7 to inform the microprocessor of the successful completion of a scan line transfer.

2.6 Scanner system control

Besides the actual transfer of image information through the scanner there are several other tasks that the microprocessor must carry out for proper operation of the scanner. In Fig 2-7 some important blocks are shown, which will be described in the following.

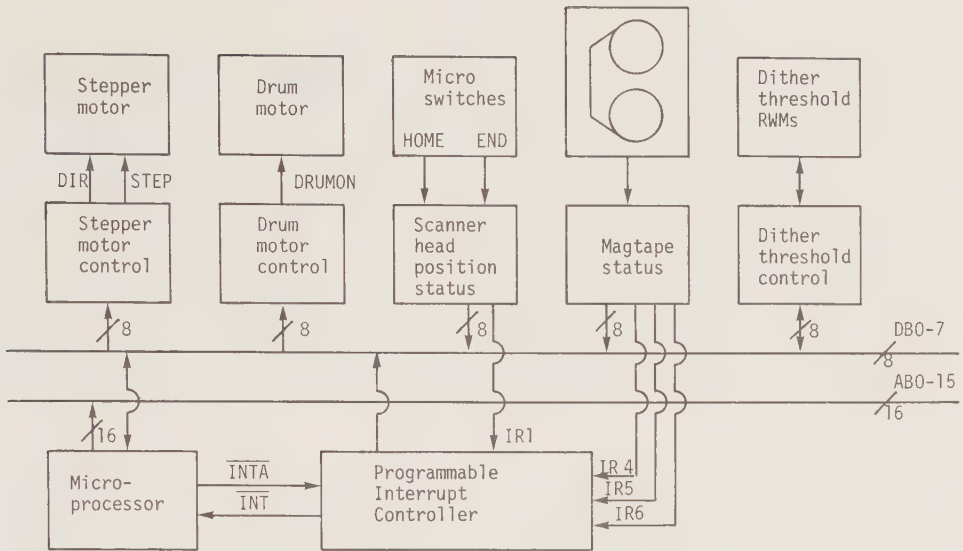


Fig 2-7 Block diagram showing the hardware used for monitoring and controlling the scanner functions. For clarity the address bus connections to the devices, such as the programmable interrupt controller, are not shown.

The scanner head is moved sideways parallel to the drum surface by means of a screw drive actuated by a stepper motor. The stepper motor is controlled from the microprocessor system through two signals, one for the stepping direction, DIR, and another for step pulses, STEP. The stepper motor requires 20 step pulses to move the scanner head 0.2 mm sideways. These 20 pulses are generated by dividing the pixel pulse signal BSTB2 with a suitable number so that every complete revolution of the drum results in an 0.2 mm movement. It is also possible to move the stepper motor without drum rotation for positioning purposes by selecting another clock generator than the BSTB2 signal.

The scanner drum is rotated by a DC pancake motor and all electronics for maintaining a constant drum surface speed are located outside the microprocessor system and hence cannot be easily controlled. Therefore the microprocessor only starts and stops the drum rotation.

Prior to the start of a scanning operation, the scanner head must be located in the start position, called HOME. This location as well as the end of the scanning area, called END, are monitored by micro-switches and the microprocessor will not start the drum rotation before it has positioned the scanner head in the HOME position.

As it is important that the scanner head movement stops when either the HOME or END position is reached, both microswitches are connected to the interrupt request line IR1. The interrupt service routine on this level will first stop the scanner head movement, thereafter determine if the scanner head is in the HOME or END position, and then take proper action according to that.

The magtape station is controlled by the microprocessor system, but its status must also be monitored. The fatal (irrecoverable) errors that can occur in the magtape station are connected with the interrupt request line IR4.

The interrupt request lines IR5 and IR6 are also connected to the magtape status circuitry. Both are used when data is read from the magtape station into the microprocessor system. Since this is never the case in the scanner applications, these interrupt service routines are not used.

The threshold technique used in the scanner to generate color shades is based on a matrix method generating alternating threshold values that are compared to the continuous tone image information after it is A/D converted (Nilsson and Nygren 1981B). The threshold values are stored in three separate Dither threshold RWMs, one for each color, and these RWMs must be loaded from the microprocessor system prior to a scanning operation. The microprocessor must also read back the threshold values from these RWMs to confirm that they are correctly loaded.

2.7 Scanner system operator communication

The only major part of the scanner system not yet discussed is shown in Fig. 2-8. Instead of using buttons to start the scanning operation, and small error lights to indicate malfunctions, the entire communication between the operator and the scanner system is carried out through a terminal. The terminal is also essential when running different utility programs for moving the scanner head, altering the Dither threshold values, etc. To be able to stop the execution of a utility program without resetting the microprocessor system, the Real Time Clock (RTC) was added. The RTC generates an interrupt request on the interrupt request line IRO every 10 ms. The service routine for this level reads the last input from the operator terminal keyboard. If it is a control-A character, generated on the terminal keyboard by simultaneously depressing both the control key and the A key, all further processing of the utility routine is aborted. This routine has a very short execution time.

3 SCANNER SYSTEM SOFTWARE DESIGN

3.1 Introduction

The scanner software was developed in close contact with the hardware design. Since a microprocessor architecture especially adopted to the present task was chosen, the software development was strongly dependent on the hardware and vice versa. This close relation will become evident in this chapter.

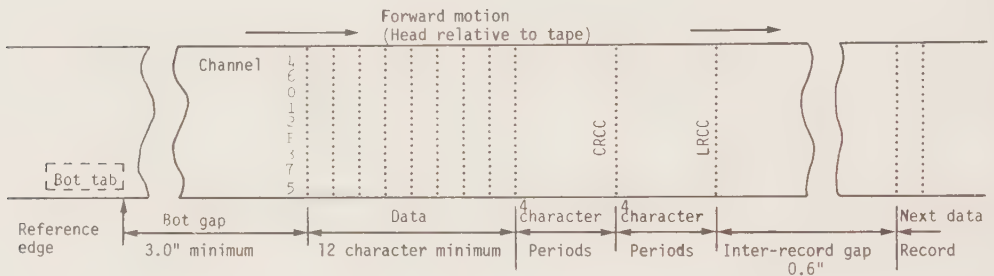


Fig 3-1 Format of 800 bpi NRZI coded 9 channel magnetic tapes. The tape is shown with oxide side up.

- * The channels 0 through 7 contains data bits in descending order of significance.
- * The channel P (parity) always contains odd data parity, i.e. the number of "1" in a 9 channel character is always odd.
- * Each bit of the LRCC (Longitudinal Redundancy Check Character) is such that the number of "1" bits in that channel including the CRCC (Cyclic Redundancy Check Character) and the LRCC is even. The LRCC will never be an all zero character, while this is possible for the CRCC.
- * An End Of File (EOF) mark is a single character record having "1" bits in channel 3, 6 and 7 for both the data character and the LRCC. The CRCC contains all zeroes. This record is separated from the previous record by 3.5" and by a normal Inter Record Gap (IRG) of 0.6" from the following record.

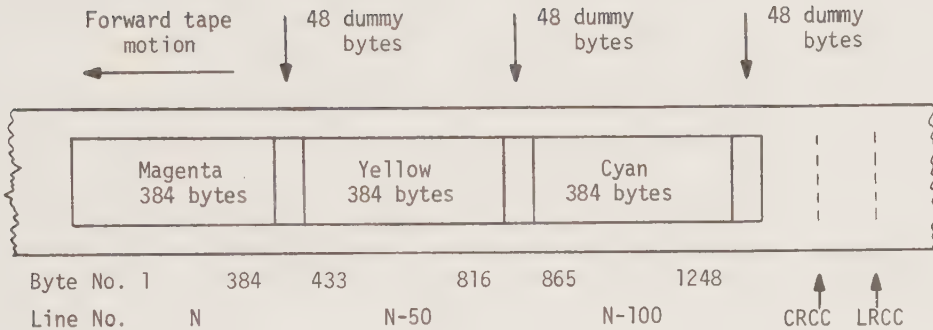


Fig 3-2 Data organization on the magnetic tape. Each record includes a total of 1296 data bytes.

First, the scanner tape format will be described as well as the software routine that performs the initiation of the scanner hardware. thereafter the chapter will focus on the subroutines that move the image data through the system and onto the magnetic tape. It should be noted that all routines, except the initiation routine, are controlled by the scanner hardware through the PIC (Programmable Interrupt Controller). Finally, the end of this chapter will deal with routines used in conjunction with normal scanning operations and routines developed in a host computer to make the generated bilevel images available for manipulation by other graphical raster system, such as COLOR and UNIRAS.

3.2 The scanner magnetic tape format

The magtape station used in the scanner system accepts 9 channel 0.5" wide computer tapes with a maximum tape reel diameter of 10.5". This is the most frequently used computer tape media today. The packing of data on tape, bpi (bits per inch), varies depending on the recording method used. In the scanner system only 800 bpi NRZI coded tapes can be produced.

The organization of image data on the tape is straight forward. All information in one scan line is registered in one record on the tape. The record also contains two error-checking characters added as shown in Fig. 3-1.

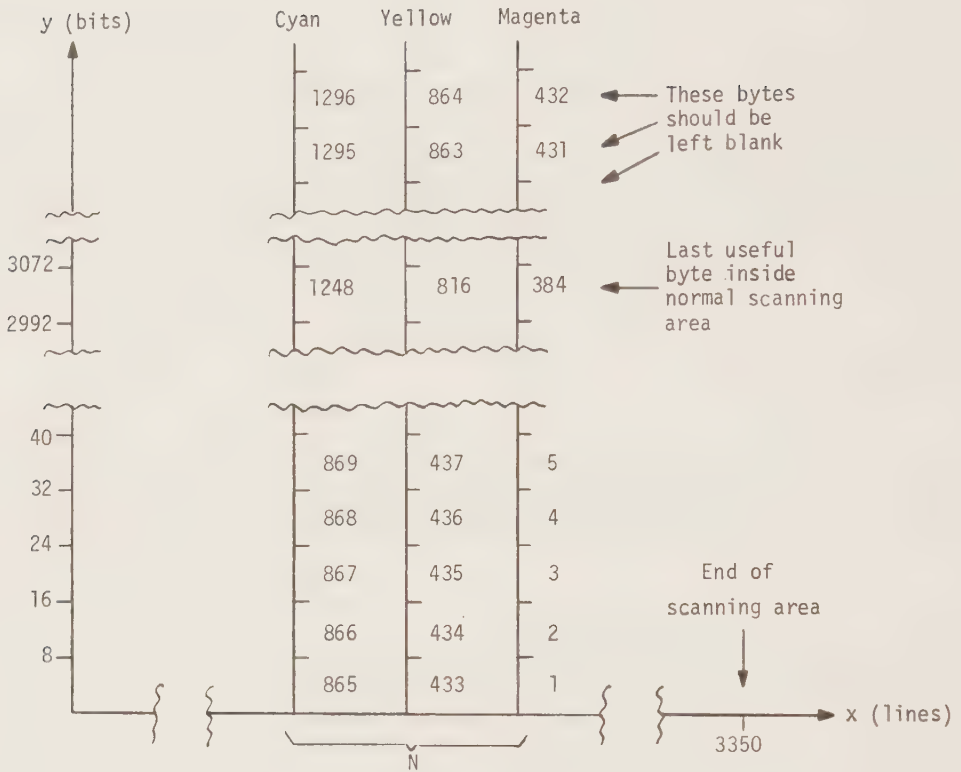


Fig 3-3 Organization of the scanning area. The three colors and their position within a record "N" on the magnetic tape are shown.

Every record on the tape is separated from the preceding and following record by an IRG (Inter Record Gap). All records together represent a file. To indicate the end of a file, a special record called EOF (End Of File) mark is added at the end. One record contains the image information for one scan line in all three colors, as shown in Fig. 3-2. The information is arranged sequentially within each of the three colors in the same order as the picture elements (pixels) are collected from the scanner drum surface as depicted in Fig. 3-3. The first magenta pixel of a scan line is stored in the MSB (Most Significant Bit) of byte 1 and the last magenta pixel of the scan line is stored in the LSB (Least Significant Bit) of byte 384. The following 48 bytes are added to fill the record with 3×3456 bits of pixel information. The reason for these dummy bytes is that the

division of 3456 by 8, 24, 32, 36 and 64 results in an integer value. This makes the tape format easily manageable in computer systems using these different word lengths.

3.3 The initiation routine

When the scanner system is started by turning the mains switch on, the microprocessor is set in an arbitrary state. As this is not recommendable, a RESET-signal for the entire system is generated by the hardware each time the power has been lost and returns again. When the reset signal ceases, the microprocessor starts executing the instruction located in memory address 0. The executing program initiates the operator terminal interface to enable the operator communication and starts the real time clock useful when executing utility programs as described in chapter 2.7. It thereafter prompts the operator that it is ready to accept commands.

At this time, all controllers, counters and ports used in the scanner system are inoperative. To initiate the scanner system and start the scanning procedure, the operator types SCAN. The microprocessor will then execute the initiation routine which sets the scanner system in a startup state. A flow chart showing the main tasks of this routine is given in Fig. 3-4. In the following, these tasks will be described.

3.3.1 The programmable interrupt controller initiation

The 8259 PIC (Programmable Interrupt Controller) has 8 different interrupt request inputs (IRO-IR7). Before it can monitor these lines for activity, two ICWs (Initial Command Words) must be received from the microprocessor. These ICWs clear all the interrupt request lines, set the PIC in the correct interrupt servicing mode for our needs and informs the PIC of the address to the memory area where the 8 different interrupt service routines begin. This memory area is $8 * 4$ bytes = 32 bytes long. The only instruction located here for each service routine is the JUMP <address> instruction. The two byte address points to the rest of the service-routine located anywhere in the memory area. The remaining byte for each of the 8 interrupt levels in the memory area is left blank.

After this initiation the PIC also requires the interrupt system in the microprocessor to be enabled for proper operation. The PIC operation will be described in chapter 3.4.

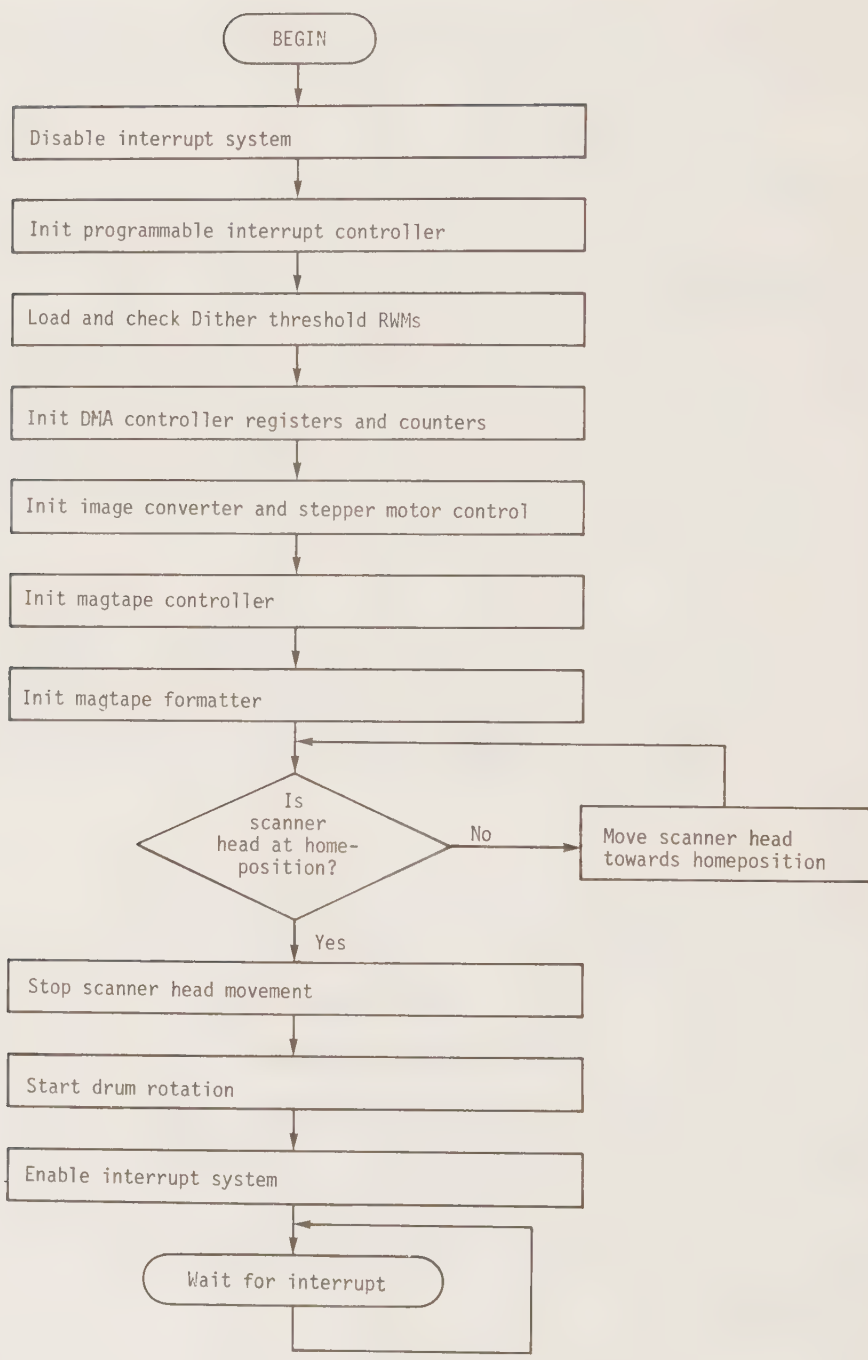


Fig 3-4 Flow chart of the scanner system initiation routine.

3.3.2 The load and check of Dither threshold RWMs

Prior to scanning, the Dither threshold values for the three colors must be moved from the microprocessor system's ordinary memory out to the dedicated RWMs located in the vicinity of the comparator circuitry. In Fig 3-5, the loading procedure of the dedicated RWMs is shown as a flow chart. A more detailed description, involving the hardware logic, is given in chapter 4.2.2.

The microprocessor system memory consists of two different memory types, RWMs and ROMs. The Read Write Memories are used for the image information and program variables that must be changed during program execution, while the Read Only Memories contain the scanner routines and utility routines which are permanently stored. The Dither thresholds could be stored in the ROM-section of the memory. However it would then be difficult to change the thresholds between the scanning operations. Therefore the RWM-section of the scanner system memory is used. The Dither threshold values to be moved to the dedicated RWMs are first loaded into the microprocessor system RWM-area through a utility routine. This routine is described in chapter 3.5.2. The threshold values can be given through a ROM inserted in a socket on the microprocessor system front panel or by manual input from the operator terminal keyboard.

After the threshold information is transferred to the dedicated RWMs, the microprocessor reads back the threshold values from the dedicated RWMs and checks that they are correct. This procedure, which is a subroutine of the loading routine, is shown as a flow chart in Fig. 3-6.

3.3.3 The DMA controller initiation

The transparent DMA controller logic is initiated directly through the hardware, as soon as the microprocessor system receives power. The part of the DMA-controller which is not initiated automatically on power up is the counter and register section. For the latter a special routine, depicted in Fig. 3-7, is used.

In this routine the "DMA memory start address"-register is set to the first RWM address where the scan line will be located. This address will be loaded into the DMA memory address counter when a block of DMA transfers shall begin. Also the "number of bytes to transfer"-counter is programmed, and given the value 1296. This value must not be reprogrammed after each complete DMA-transfer, as it is kept by the counter and internally reloaded for each new block of DMA transfers.

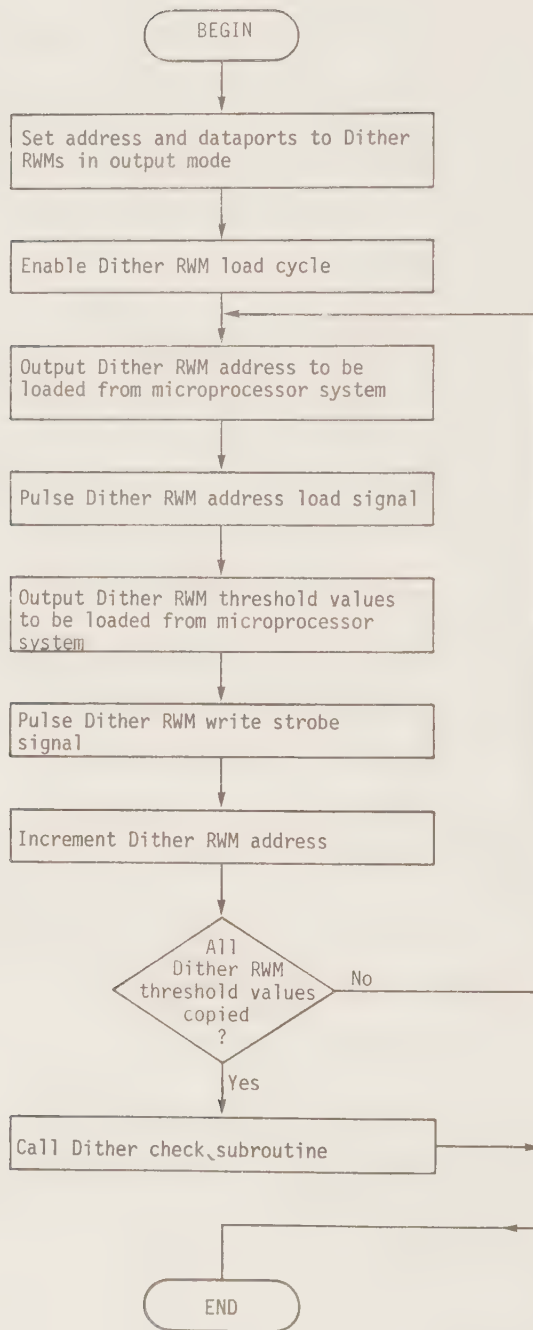


Fig 3-5 Flow chart of the Dither threshold RWM load routine

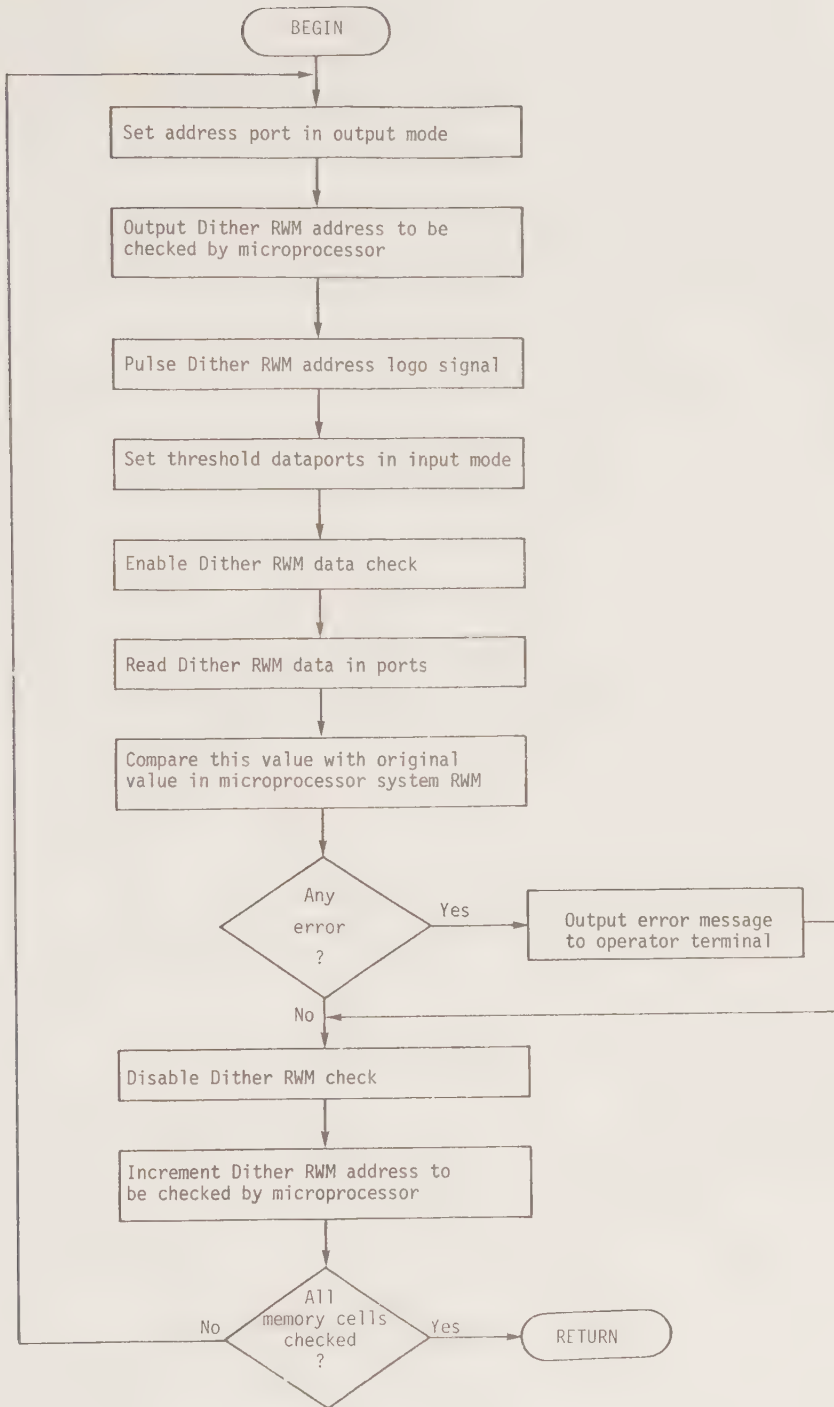


Fig 3-6 Flow chart of Dither threshold RWM check subroutine.

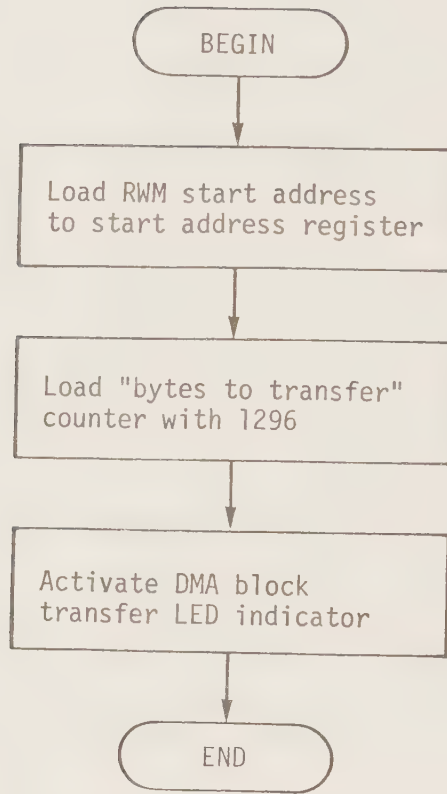


Fig 3-7 Flow chart of the DMA controller register and counter initiation.

Also a visual indicator, in the form of a yellow LED (Light Emitting Diode) mounted on the scanner system front panel, is initiated. It will blink for each new block of DMA-transfers.

The DMA controller is thereafter ready for the first transfer and can be started by the single instruction, OUT 01.

3.3.4 The image dataports and stepper motor control initiation

In Fig 3-8 a flow chart showing this part of the initiation routine is given. The image information from the optical scanner head must be moved from the serial to parallel converter 2 (S/P2) to the RWM by the microprocessor. Therefore the three 8-bit ports located in S/P2 are programmed to transfer data into the microprocessor system.

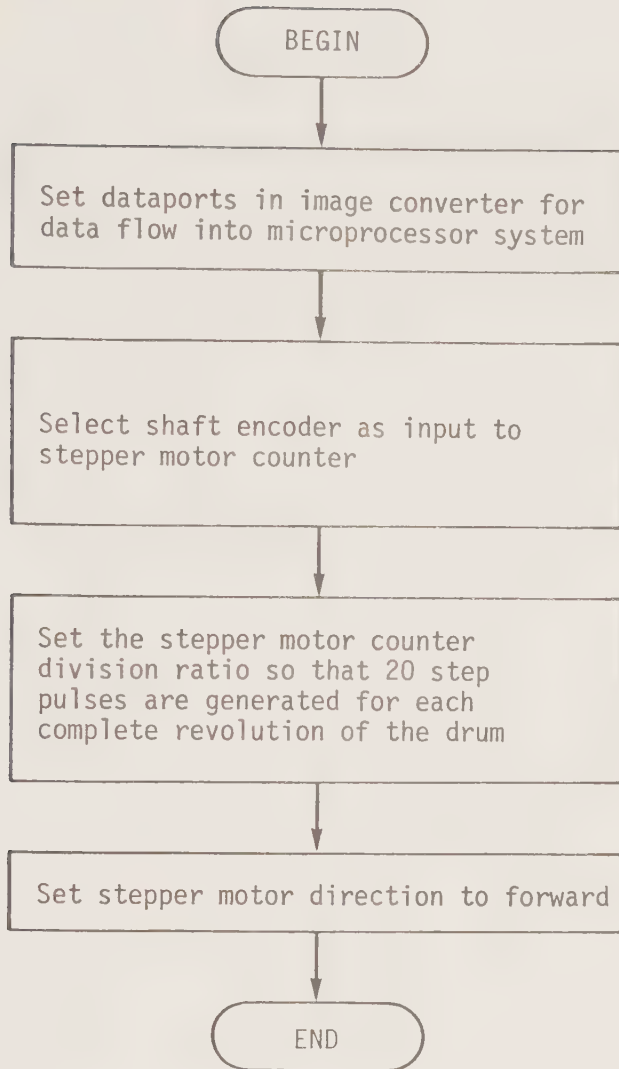


Fig 3-8 Flow chart of the image dataports and stepper motor controller initiation routine.

For each revolution of the drum, the optical scanner head must be moved sideways to the next scan line to obtain new image information. This movement is carried out by a stepper motor turning a lead screw onto which the scanner head is fastened. This sideways movement is synchronized with the drum rotation through the shaft encoder mounted on the drum axis. The shaft encoder delivers 3360 pulses per revolution on one channel and 1 pulse per revolution on another. The 3360 pulses are divided in a programmable prescale counter so that only 20 pulses will be generated for the stepper motor for each complete revolution of the drum. As the scanner head moves 0.01 mm for each step of the stepper motor, this results in a 0.2 mm movement. In some cases it is necessary to move the scanner head although the drum is not rotating. Therefore an alternate pulse generator can be selected through software. Its frequency is much higher, and consequently the prescale counter must be reprogrammed when it is used.

3.3.5 The magtape controller and formatter initiation

The initiation procedure of the magtape controller and formatter is shown as a flow chart in Fig. 3-9. The magtape station is set in write mode by the magtape controller. Thereafter several parameters must be given to the magtape formatter so that the transmission of data from the formatter to the magtape station will be correct.

The tape transport speed must be known to the formatter to ensure that the data transferred to the magtape station is written at the correct speed. During a normal write operation several delays must be known and/or controlled by the formatter. First there must be a delay between the "move tape forward"-command and the actual transfer of the first data byte to the tape. During this delay the tape is accelerated to its nominal speed. After the last byte in a record is written onto the tape, there must be a delay before the tape motion is stopped, "write-stop delay". There is also a delay between the "stop tape movement"-command and the actual stop of the tape motion. These delays are specified, or can be derived from the manufacturer's service manual (Pertec Inc.).

When all delays are defined in the formatter, the magtape controller checks the magtape status registers to see that everything is correct. If this is true, the tape is advanced 3 " forward from the tape load point, as specified by the manufacturer, cf. Fig 3-1.

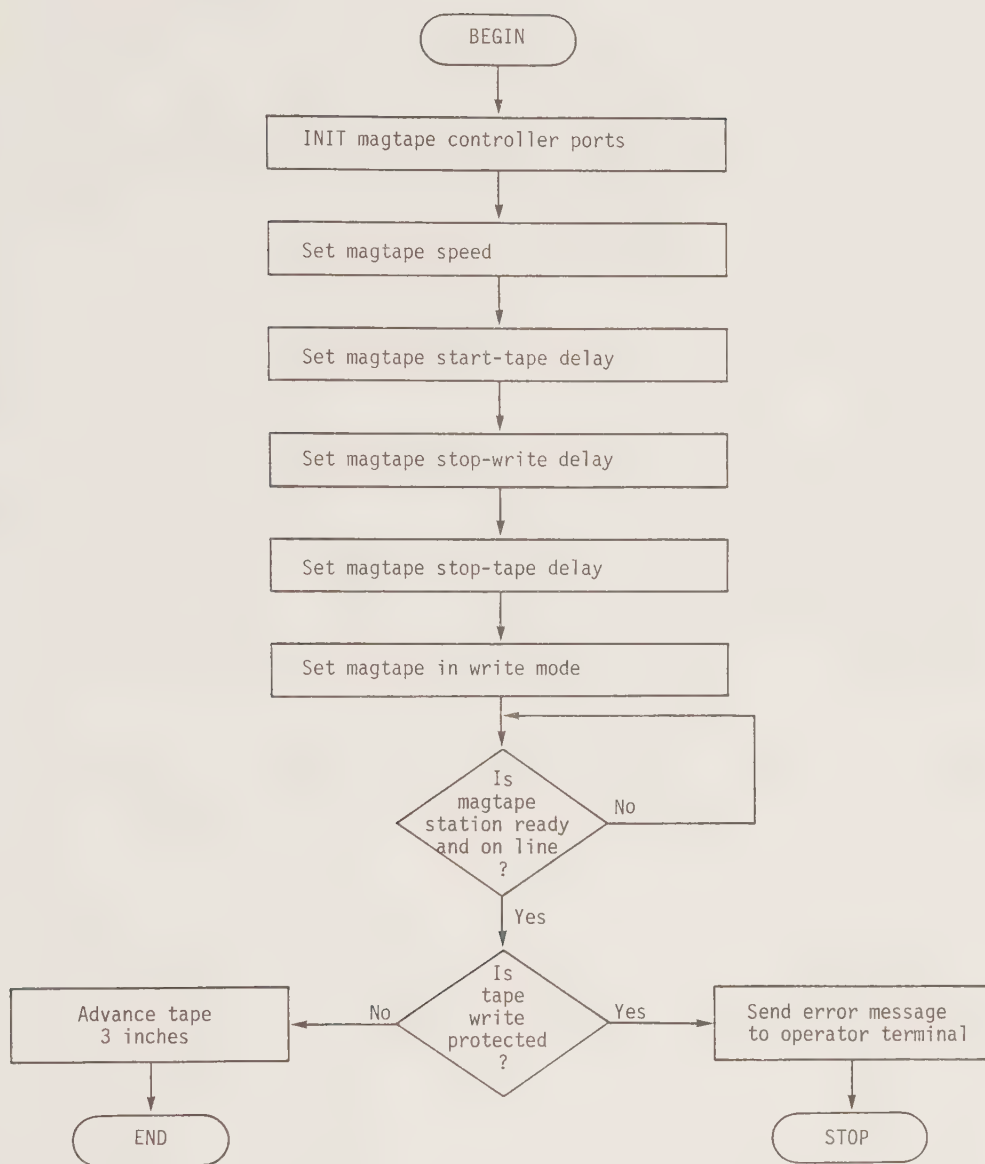


Fig 3-9 Flow chart of magtape controller and formatter initiation routine.

3.3.6 The termination of the initiation routine

At this point in the routine, all counters, ports and controllers are ready for operation. But before the scanning operation starts, the scanner head must be in the start position called HOME and the drum must be rotating. A detailed flow chart of this latter part of the initiation routine is given in Fig. 3-10.

The microprocessor checks the HOME-position microswitch. If the scanner head is not present, the stepper motor is started to move it there.

To start the stepper motor when the drum is not rotating requires another STEP-pulse generator. This alternate frequency is obtained from the 2 MHz microprocessor system clock. As this frequency is much higher than the frequency normally received from the shaft encoder, the prescale-counter must be reprogrammed with a larger number. By slowly decreasing this number during stepping, the stepper motor is accelerated to a speed which is much higher than normal. The scanner head therefore reaches the HOME-position in a short period of time.

With the scanner head in the HOME-position, the drum motor is started. As it takes some time for the drum to reach a constant speed, the microprocessor executes a delay routine for approx. 5 seconds before the last task of the initiation routine is carried out.

The first interrupt service routine to be executed in the actual scanning operation is the "next scan line"-routine. To be sure that no other interrupt service routine is executed, except the RTC (Real Time Clock) routine which has no effect on the scanning procedure, an Interrupt Mask Register (IMR) in the PIC is set to disable all other levels than the "next scan line"-routine level. Thereafter all interrupt request lines are cleared, and the interrupt system in the microprocessor is enabled. On the next scan line-pulse (SLSTB), from the shaft encoder, the PIC activates the "next scan line"-routine and from here on the entire scanning operation is controlled by the PIC.

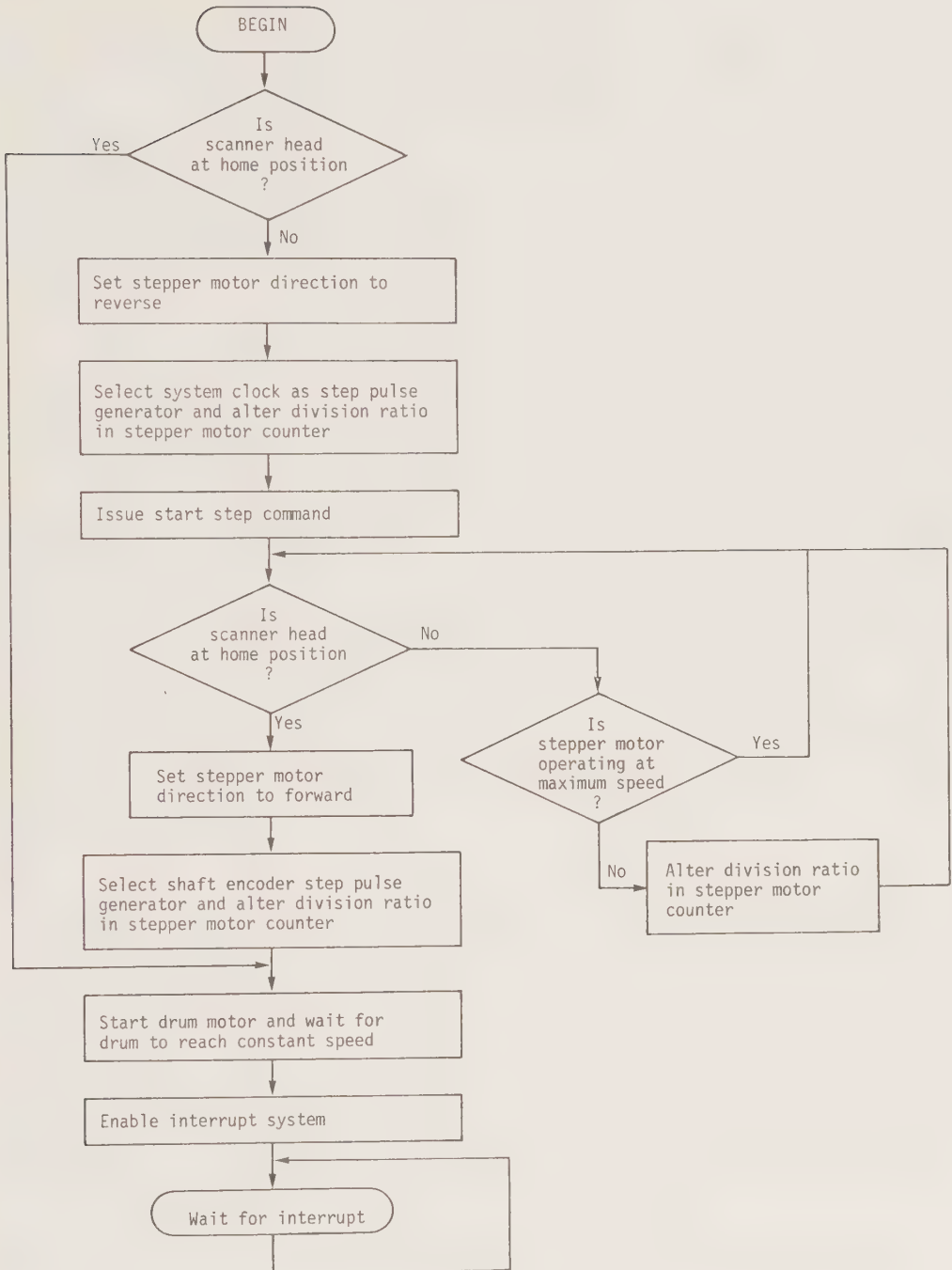


Fig 3-10 Flow chart of the termination of the scanner system initiation routine.

3.4 The programmable interrupt controlled routines

3.4.1 Function of the programmable interrupt controller

As pointed out earlier in this report, the entire scanning operation is controlled by hardware events through the programmable interrupt controller (PIC). Therefore, before the different interrupt routines are described in detail, the PIC and its interaction with the microprocessor will be discussed.

The 8259 PIC is shown in Fig. 3-11. It can accept 8 levels of interrupt requests, IRO-IR7, the number of the level determining its priority. For expandability it has built-in features to accept up to 64 levels using additional PICs. The interrupt requests received at the IR input lines are handled by two registers in cascade, the Interrupt Request Register (IRR) and the In Service Register (ISR). The IRR is used to store all the interrupt levels which are requesting service, and the ISR is used to store all the interrupt levels which are being serviced. Several levels can be serviced simultaneously at any given time. If a level with higher priority issues an interrupt and the interrupt system in the microprocessor is enabled, the current level will be suspended, and the ISR will indicate both levels as being serviced. To disable interrupts on any interrupt level, an 8 bit Interrupt Mask Register (IMR) is included in the PIC. By setting a bit in the IMR, the corresponding interrupt request line cannot cause an interrupt. This masking has no effect on the priority among the other levels.

The PIC has several features that are dynamically selectable and changeable under software control. Several of these features are not used in the scanner system. The following description shows the operational function of the PIC in the scanner system with the appropriate ICWs (initial Command Words) received from the microprocessor and the interrupt system in the microprocessor enabled.

1. One or more of the interrupt request lines IRO-IR7 are raised high, setting the corresponding IRR bit(s). The IRR acknowledges a positive going edge only.
2. The PIC accepts these requests, resolves the priorities - IRO first and IR7 last - and sends an INT-signal on a dedicated line to the microprocessor.
3. The microprocessor finishes the execution of its present instruction and thereafter acknowledges the INT-signal with an INTA-pulse on another dedicated line.

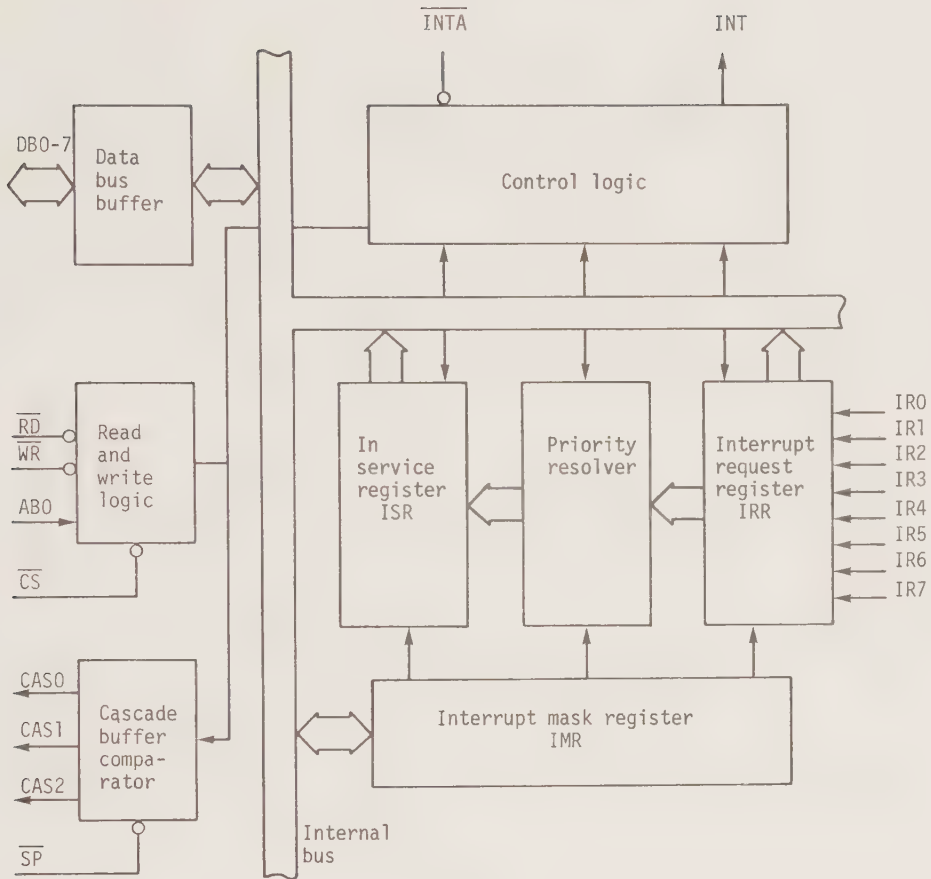


Fig 3-11 Block diagram of the 8259 Programmable Interrupt Controller (PIC).

4. Upon receiving an $\overline{\text{INTA}}$ pulse from the microprocessor, the highest priority ISR bit is set, and the corresponding IRR bit is reset to enable new interrupt requests on this priority level. The PIC will also release a CALL instruction code <1100 1101> onto the 8 bit data bus through its DB0-7 pins.
5. This CALL instruction will initiate two more $\overline{\text{INTA}}$ pulses to be sent to the PIC from the microprocessor.

6. These two additional $\overline{\text{INTA}}$ pulses allow the PIC to release its preprogrammed service routine address onto the data bus. The lower 8-bit address at the second $\overline{\text{INTA}}$ pulse and the higher 8-bit address at the third $\overline{\text{INTA}}$ pulse.
7. This completes the 3-byte CALL instruction released by the PIC. The microprocessor has automatically pushed the program counter value of the program it was executing prior to the CALL instruction on the stack so that it can resume execution of this program after the interrupt service routine is ended.

The stack is the microprocessor's scratchpad. It is physically a part of the RWM, and usually located near the upper end of it. Besides program counter values, the stack is also used for temporary storage of microprocessor register contents.

The microprocessor has a dedicated 16-bit register, SP, pointing at the last occupied cell in the stack. For every PUSH onto the stack, the SP register is decremented, and for every POP off the stack, the SP register is incremented. It is essential that the PUSH and POP instructions are balanced, otherwise the stack will grow uncontrollably into other vital parts of the executing program.

8. The ISR bit is not reset until the EOI (End Of Interrupt)-command is issued from the microprocessor to the PIC. This is normally taken care of at the end of the interrupt service routine.

The use of different priority levels in the interrupt controller, as shown in table 3-1, is chosen according to the importance of each event, e.g. if the END position of the scanning area is reached, there is no need to continue moving image information through the scanner system.

In the following description, the interrupt service routines will be arranged the same way as they are used when image information flows through the system. The RTC interrupt service routine on level IRO will not be described as it is only used in the utility routines. For the same reason, the interrupt service routines on level IR5 and IR6 will not be discussed.

- IR0 Real time clock interrupt level. This level is activated from a 8253 PIT (Programmable Interval Timer) located on the magtape formatter board every 10 ms.
- IR1 HOME and END position indicator interrupt level. This level is activated by the microswitches located in the HOME and END positions of the scanner head.
- IR2 Pixel strobe interrupt level. This level is activated every time 8 pixels in all three colors are ready for transfer from S/P2 to the RWM.
- IR3 Next scan line interrupt level. This level is activated by the SLSTB (next Scan Line STroBe) pulses from the shaft encoder, which occurs once every complete rotation of the drum.
- IR4 Magtape station interrupt level. This level is activated when the magtape status port receives a fatal error condition signal from the magtape station.
- IR5 Magtape parity error interrupt level. This level is activated from the magtape formatter board if a parity error is detected when reading from the magtape station.
- IR6 Magtape gap detect interrupt level. This level is activated from the magtape formatter board when an IRG (Inter Record Gap) is detected while reading from the magtape station.
- IR7 DMA transfer completed interrupt level. This level is activated by the magtape formatter when a complete scan line has been successfully transferred to the magtape station, and stored on the tape.

Table 3-1 The use of the different interrupt levels in the Programmable Interrupt Controller (PIC).

3.4.2 The pixel strobe interrupt service routine

This interrupt service routine is the most frequently used routine in the scanner system. The IR2 signal is activated by every 8th bit (pixel) strobe and hence executed more than 400 times during one revolution of the drum. It only performs one task, moving image information packed as bytes from S/P2 to the RWM. The flow chart in Fig. 3-12 shows this function in greater detail.

Before any image information is moved, a check is made to make sure that the information will be placed within the allocated scan line area in the RWM. To transfer the image information to the correct memory locations, the RWM cell called PRESENT, always contains the address of the last occupied cell in the magenta part of the scan line in RWM. The cell called PRESENT is given a new start address by the "next scan line" interrupt service routine and thereafter incremented in this routine for each transfer. As the image information must be stored the same way in the RWM as on the magtape, the yellow and cyan bytes are stored with an offset of 432 and 864 bytes respectively from the address given in cell PRESENT, c.f Fig 3-2.

Before leaving this routine, the EOI-command is issued to the PIC and the interrupt system is enabled.

3.4.3 The next scan line interrupt service routine

This interrupt service routine is called once for each complete revolution of the drum. The IR3 signal is activated by the SLSTB pulses from the shaft encoder. It has four main functions to carry out:

1. Give start address in RWM of scan line N-1 to the DMA controller start address register.
2. Give start address in RWM of scan line N to a memory cell, called PRESENT, This memory cell is used by the pixel strobe interrupt service routine when storing the new scan line in RWM.
3. Check that the previous DMA-transfer (if any) was successful by reading the contents of memory cell DMAOK. The memory cell DMAOK is given a positive value by the DMA transfer completed interrupt service routine if the DMA transfer was successful.
4. Start the DMA transfer of scan line N-1.

A flow chart showing these functions is given in Fig. 3-13.

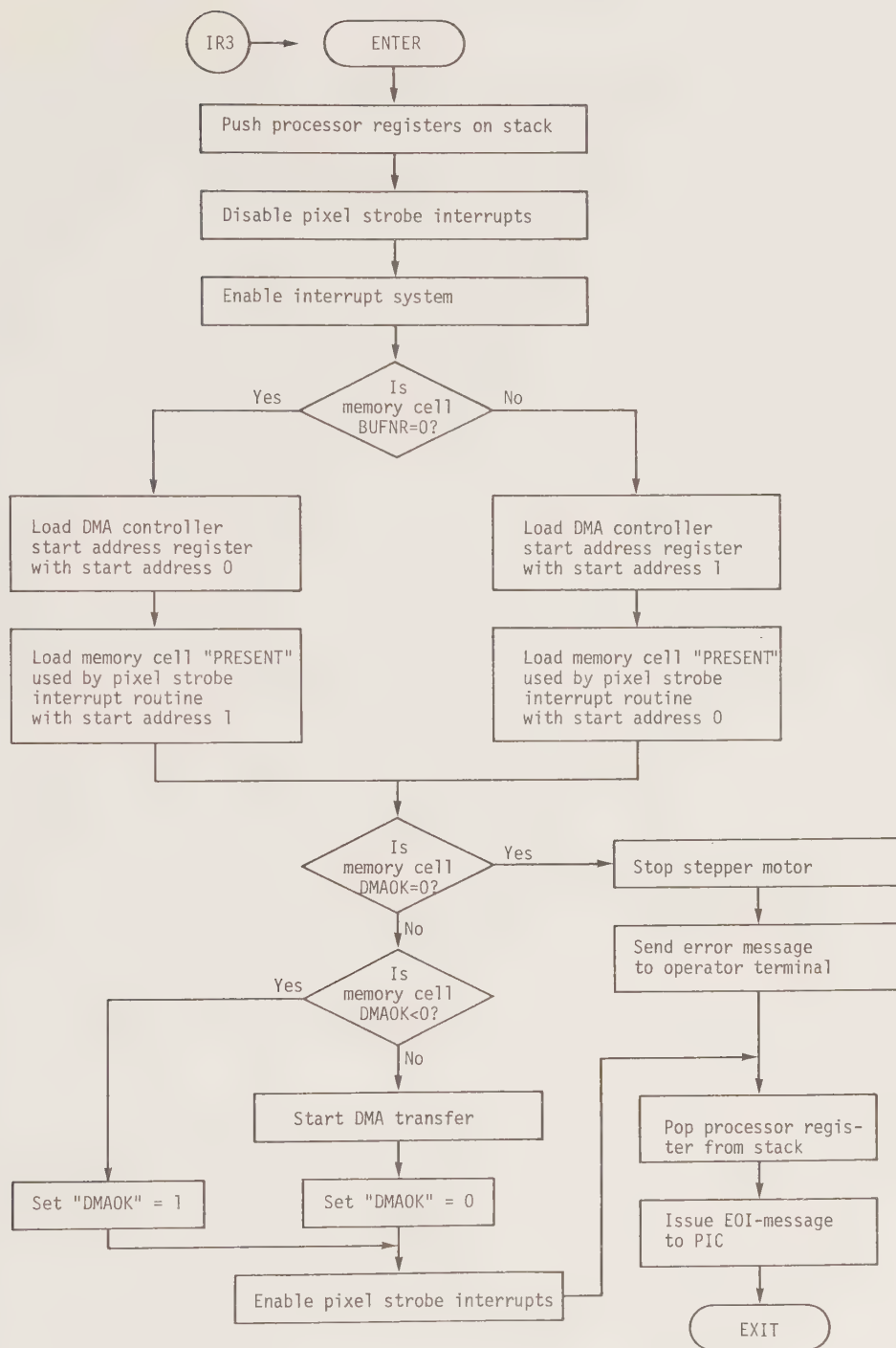


Fig 3-12 Flow chart of the pixel strobe interrupt service routine.

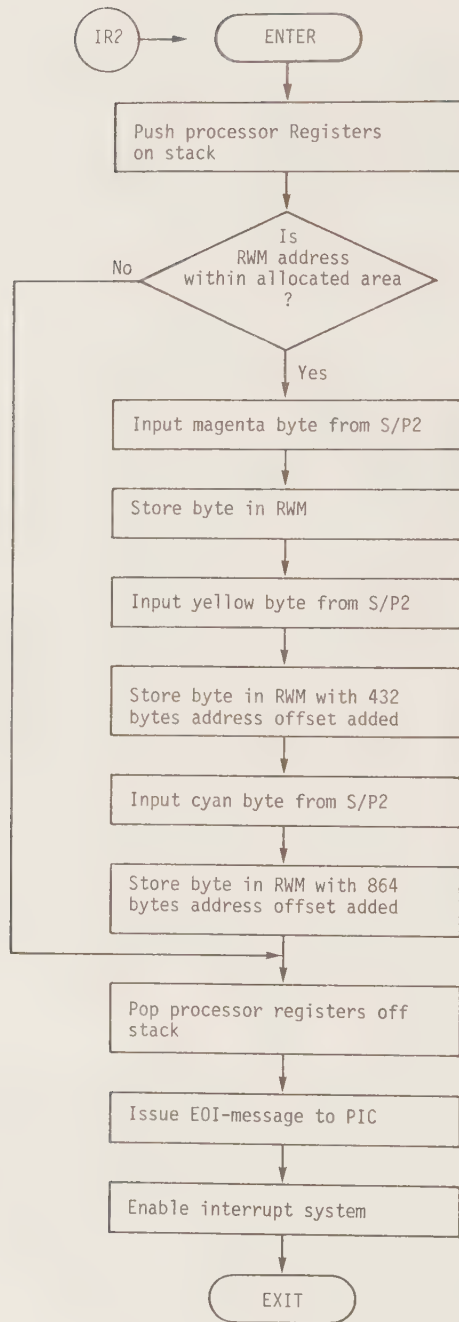


Fig 3-13 Flow chart of the next scan line interrupt service routine.

While the microprocessor is moving scan line N into the RWM, the DMA controller is moving scan line N-1 out from the RWM. This occurs concurrently and therefore enough space for two scan lines must be allocated in the RWM. The "next scan line" interrupt service routine uses a memory cell called BUFNR in the RWM to know in which of the two preassigned address ranges the next scan line shall be placed. This also gives the start address for the DMA transfer of scan line N-1. The DMA controller and the RWM cell PRESENT are given one of the addresses each. As mentioned earlier, the "number of bytes to transfer"-counter in the DMA controller must not be reloaded from the microprocessor until the number of bytes to transfer is altered. Hence the DMA controller is ready for a transfer after receiving the new RWM address.

Before this transfer is started, a RWM cell called DMAOK is checked. This cell informs the routine if the previous DMA transfer was successful or not. If the cell is nonzero, the previous transfer was OK. If the cell is positive, a new transfer shall take place. If the cell is negative, which it always is the first time this routine is executed and no previous scan line exists, no DMA transfer shall take place.

The start of the DMA transfer is a simple OUT 01-instruction, which loads the DMA controller memory address counter with the DMA transfer start address, internally reloads the "number of bytes to transfer"-counter with 1296, starts the magtape formatter timing sequence and makes the first DMA-request, DMACKE (DMA Clock Enable). All consecutive DMA-requests will be generated by the formatter hardware.

Before leaving the service routine, the EOI-command is given to the PIC and all other relevant interrupt request levels are enabled.

If there was an error in the previous DMA transfer (DMAOK=0), the stepper motor is stopped, an error message is sent to the operator terminal and thereafter the scanning operation continues on the next "next scan line"- interrupt request.

As the stepper motor is stopped, there is plenty of time to reverse the tape to the beginning of the erroneous record and rewrite it again. This facility is not implemented in the present software, mainly because DMA transfer errors have never occurred during normal scanning operations.

Before leaving the routine after an error, the EOI-command is given to the PIC and no other interrupt request levels but the present are enabled.

3.4.4 The DMA transfer completed interrupt service routine

This interrupt service routine is executed once for every revolution of the drum. The IR7 signal is activated by the magtape formatter when the transfer of a scan line is completed and the information is stored on the tape. It is a very short service routine that sets the RWM cell called DMAOK to a positive value. The flow chart in Fig. 3-14 shows the function.

The purpose of this interrupt service routine is to reduce the execution time of the "Next scan line" interrupt service routine by making the control of "previous DMA transfer completed" a mere check of a RWM cell.

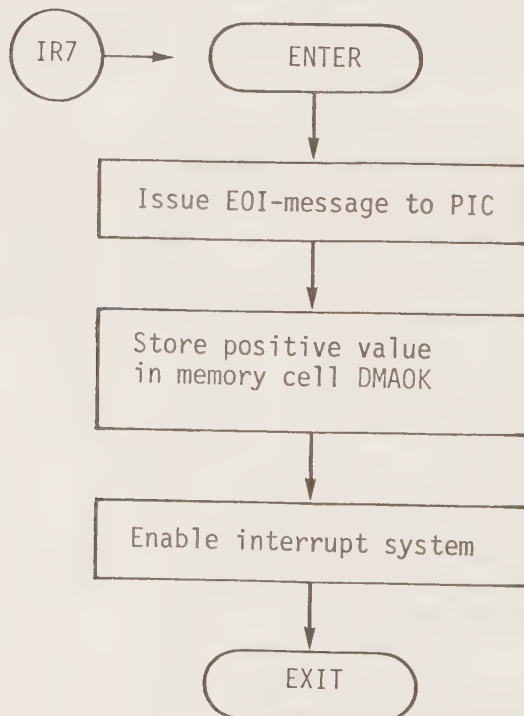


Fig 3-14 Flow chart of the DMA transfer completed interrupt service routine.

3.4.5 The HOME and END position interrupt service routine

This interrupt service routine is called twice at the end of a completed scanning operation. The IRI signal is generated by the microswitches located at the HOME and END positions of the scanner head. It performs two tasks: it alters the stepper motor stepping direction at the end of the scanning area and terminates the entire scanning operation at the home position. A flow chart showing the function of this routine is given in Fig. 3-15.

The present interrupt service routine is normally activated the first time when the scanner head reaches the END position. After this routine has determined that it is the END indicator causing the interrupt, all interrupt request levels used by the scanner system except the present are disabled. Thereafter the drum motor is stopped and the STEP pulse to the stepper motor from the shaft encoder ceases. Instead the system clock is selected as STEP pulse generator, the stepping direction reversed and the stepper motor accelerated to a higher speed compared with its speed during the scanning operation. An EOF-mark is written on the magtape and the magtape station can be switched manually offline and rewound, if no more images shall be recorded on the tape after the present image file.

Before the service routine is ended, the EOI-command is issued to the PIC, and the interrupt system is enabled. The only interrupt request affecting the scanner operation that can be acknowledged is the HOME position interrupt request.

The second time this interrupt request service routine is activated is when the scanner head reaches the starting position for the next scanner operation. Then the HOME position microswitch activates IRI, the stepper motor stops and this routine reads a port to determine which of the two indicators is active. As it is the HOME indicator, no further processing is carried out.

This terminates the scanning session, and the tape can be moved to a host computer for additional computations in a graphic color raster system, or moved to the ink jet plotter for plotting. If all colors shall be plotted, the image must be processed in a host computer to cope with the color offset in the plotter due to the physical layout of the ink jets.

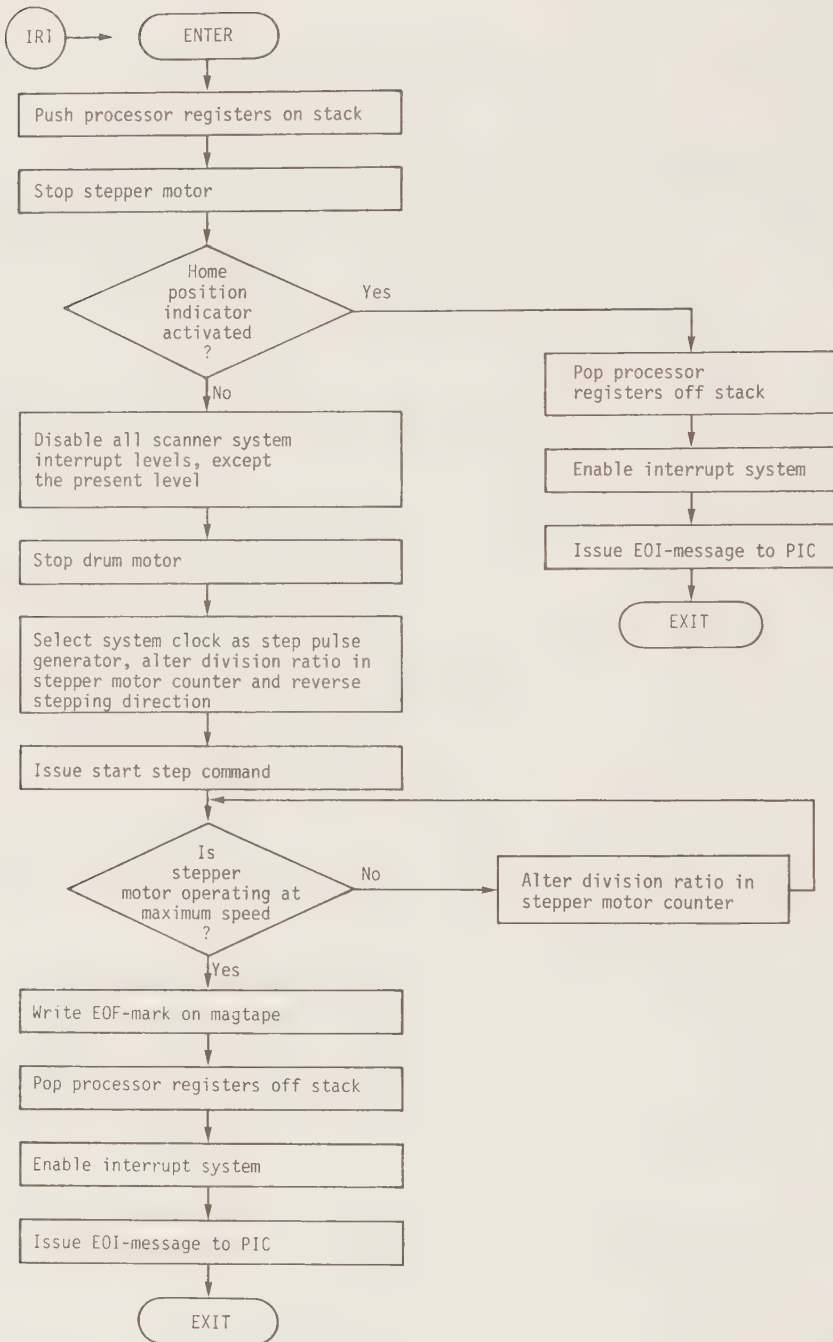


Fig 3-15 Flow chart of the HOME and END position interrupt service routine.

3.4.6 The magtape station error interrupt service routine

This interrupt service routine is normally never used during the scanning operation. But if something goes wrong in the magtape station it will be activated.

Presently three signals from the magtape station are connected to the PIC. They are the ONL, RNG and EOT signal, and any one of them can cause an interrupt request on this level. The three signals monitor the following functions:

ONL = ONLine, checks that the magtape station is connected to the scanner system and can receive commands and data from the controller and formatter.

RNG = RunniNG, checks that the tape is running.

EOT = End Of Tape, checks that the end of tape, marked with a reflective spot on the magtape, is not reached.

In the present version of this interrupt service routine, the only action taken when an error occurs is sending an error message to the operator terminal, as the flow chart shows in Fig. 3-16. This error message is adequate for most cases as these errors require operator intervention, and the image must be scanned all over again.

3.5 Utility routines within the scanner system

As the scanner system is a prototype, several extra utility routines for program development are installed. It is not the intention of this report to discuss these utility routines as they are not used in conjunction with normal scanner operations. Instead two routines frequently used prior to a scanner operation will be described.

3.5.1 The scanner head positioning routine

This routine is especially useful when adjusting the DC-offset and amplification of the analog amplifiers. The scanner head is moved to different positions across the image and measurements are carried out. An ordinary voltmeter is used for static measurements, i.e. when the drum is not rotating, and an oscilloscope is used for dynamic measurements, i.e. if the drum is rotating.

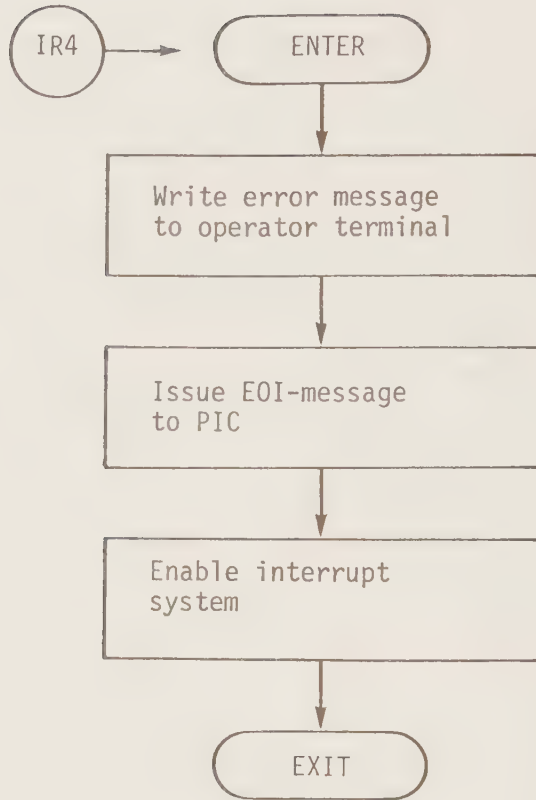


Fig 3-16 Flow chart of the magtape station error interrupt service routine.

The scanner head positioning routine, which is depicted as a flow chart in Fig. 3-17, is controlled through the operator terminal. Only three codes are accepted from the terminal keyboard, <01>, <08> and <1F> (in hexadecimal notation). The corresponding keys on the operator terminal vary from one manufacturer to another, as two of the codes are non-standard ASCII-codes.

On the Teletec terminal most frequently used with the scanner system, the keyboard keys are marked as follows;

01 : ESC
 08 : <--
 1F : -->

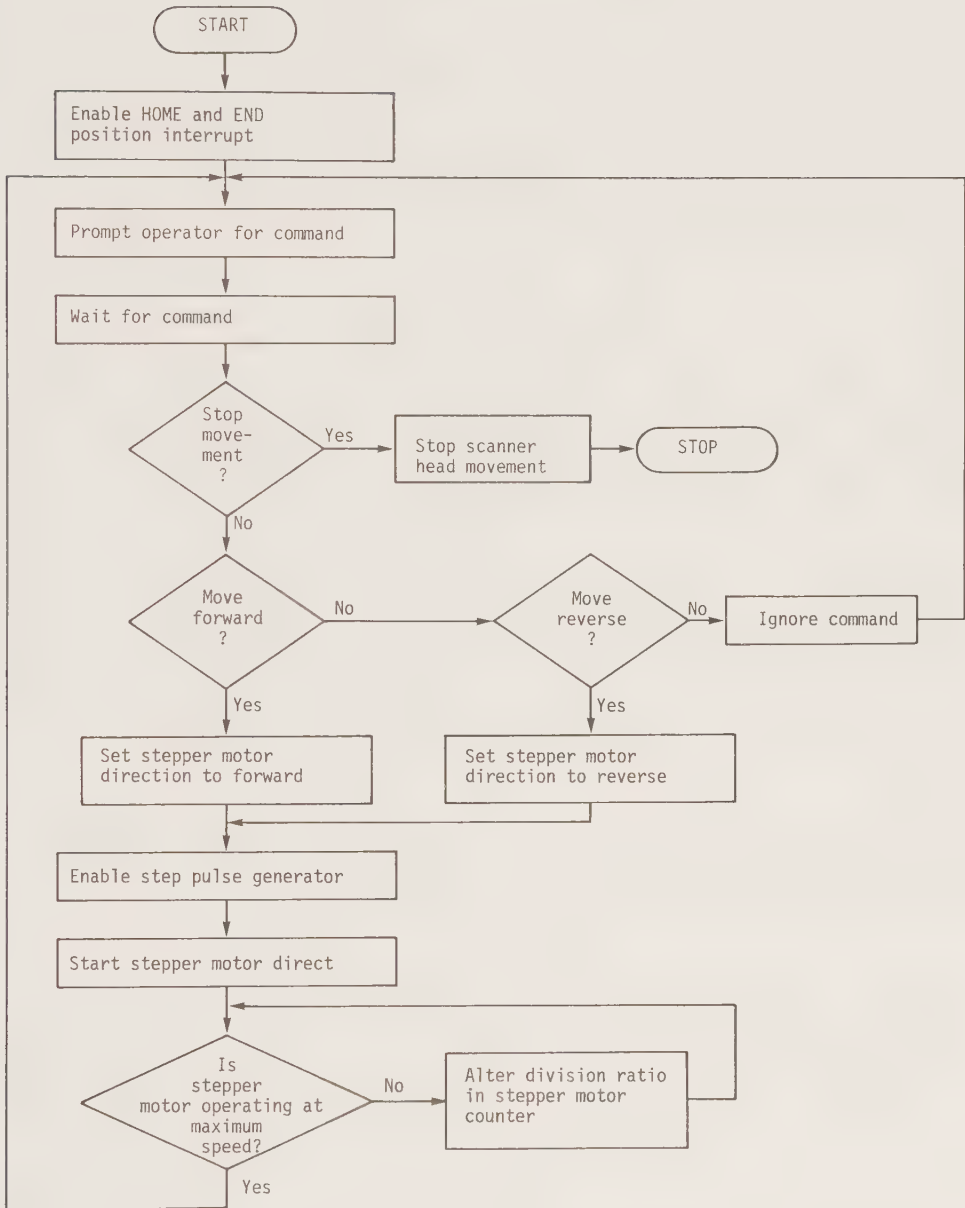


Fig 3-17 Flow chart of the scanner head positioning routine.

The arrows, normally used for cursor movement, control the direction of the scanner head movement while the ESC-key halts the scanner head and terminates the routine.

There is one flaw in this routine which makes short movements < 10 mm impossible. The operator terminal keyboard is not monitored during the acceleration of the stepper motor, and hence the stepper motor cannot be controlled during this time interval. As a quick movement to a desired area rather than precision positioning was the aim of this routine this flaw has not been corrected.

3.5.2 The Dither threshold preload routine

When a scanning operation is started, the Dither threshold matrix RWMs are loaded with threshold values from the microprocessor system RWM. The default value loaded into every threshold matrix position is 128. This threshold value is used for generation of black and white images when no gray tones are required.

In all other cases, when color shades or gray tones are wanted, the threshold values for the Dither threshold RWMs must be placed (preloaded) into the microprocessor system RWM beginning at address location 7F12 and ending at address location 7FD1 (in hexadecimal notation) prior to the execution of the scanner system initiation routine. A flow chart showing the routine functions is given in Fig. 3-18.

The Dither threshold preload routine, was primarily not intended for this purpose. The routine was developed by Olle Hydbom, a former employee of the Department to be used with the EPROM-programmer, but as it turned out it can also be used for this purpose.

This routine can handle transfers of data from an EPROM (Erasable Programmable Read Only Memory) inserted in a socket located on the front panel of the microprocessor system into the RWM. The routine can also manage transfers of threshold values from the operator terminal into the RWM, although this is a tedious task for the operator to handle.

In normal operation, the use of different threshold matrices is limited to a few. Therefore this routine can be replaced by an additional ROM containing all these threshold matrices. This would also reduce the hardware necessary for scanner operations, as the EPROM-programmer becomes obsolete.

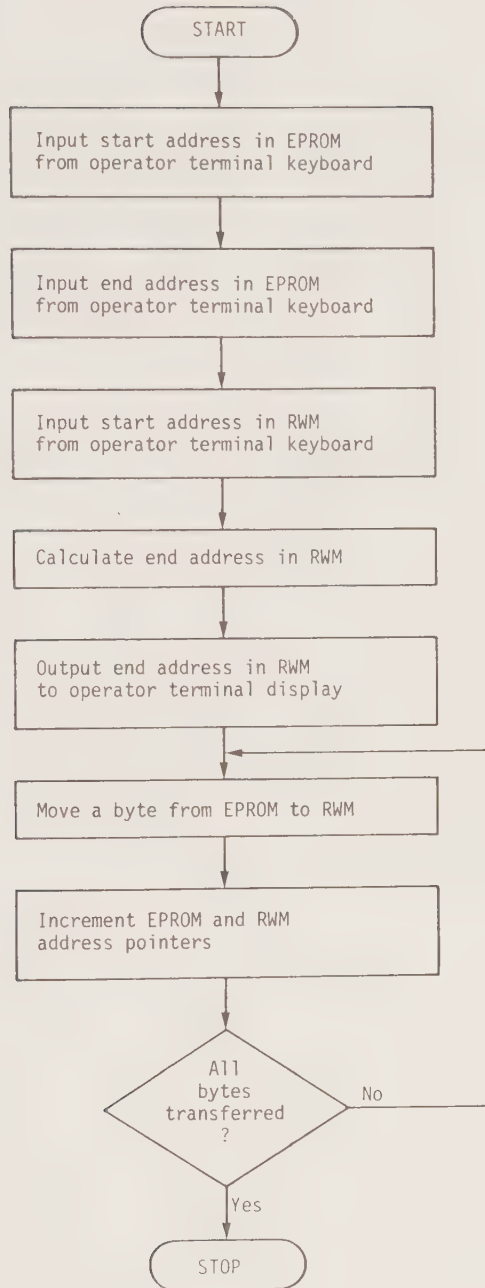


Fig 3-18 Flow chart of the Dither threshold preload routine.

3.6 Related routines in a host computer system

For the scanner system software development a Data General Nova 2.10 minicomputer was used. All routines were entered from a terminal and stored on the minicomputer system disc memory. The routines were all written in Intel standard assembler and translated into executable machine code for the 8080A microprocessor by a cross assembler program in the minicomputer.

The machine code was thereafter transferred through a serial communication link to the microprocessor system. To designate the end of a transfer, the communication routine in the minicomputer system added the character string 'ABCDEF'. This string was recognized by the microprocessor system as an EOF (End Of File) mark. The serial link could operate in both directions, and hence the minicomputer system was used to save copies of the software development carried out in the microprocessor system.

During normal scanning procedure, the scanner system has no contact with the minicomputer until the magtape is manually transferred from the scanner system to the minicomputer system. In the following two routines developed for entering the scanner images into color raster systems such as COLOR, UNIRAS and MULTIRAS will be given.

3.6.1 Routines for entering the scanner image into a software raster system

The bilevel image from the scanner is stored on the magtape, scan line by scan line. In the software raster systems mentioned above, the information is stored as small rectangles.

The INSCAN routine transforms the tape information into suitable rectangles for the raster software systems, at the same time as it moves the information from the magtape over to the minicomputer system disc memory. The same routine is also used for transferring the image information from the disc memory back to the magtape. This latter transfer accepts an offset between the three colors to suit different output media, e.g. 50 lines offset for the Applicon Ink Jet plotter.

With the image information stored on the disc memory, additional data can be added through the software raster systems mentioned above. In some cases the additional information must be positioned on the scanner image. To meet this requirement the SCANMEASURE-routine adds a 10 mm grid net to the scanner image. All calculations for correct positioning can be carried out on an extra test plot of the scanner image overlaid with this grid net.

4. SCANNER SYSTEM HARDWARE DESIGN

The scanner system consists of several parts which interacts with one another as shown in Fig. 4-1. The scanner software has already been described, and the analog circuitry is described in Nilsson (1981). The remaining parts are the optical scanner section and the micro-processor system with it's different interfaces and associated circuitry. In the following, these parts will be described.

4.1 Mechanical hardware

The hardware necessary for the scanner can be divided into a mechanical and an electrical/electronic part. The borderline between them is somewhat difficult to draw. The intent of this report is not to describe the mechanical construction, as it is similar to that of the color ink jet plotter described by Bladh (1982). Only those mechanical parts that are of interest when describing the scanner system will be mentioned.

In Fig. 4-2 the basic units of the color image scanner are shown. The drum motor, stepper motor and shaft encoder are the three vital connections between the mechanical hardware and the electrical/electronic hardware. The drum motor rotates the drum with the shaft encoder mounted on the axis. The shaft encoder delivers electrical pulses to the drum motor control to maintain a constant drum surface speed, and the stepper motor normally also receives stepping pulses from the shaft encoder.

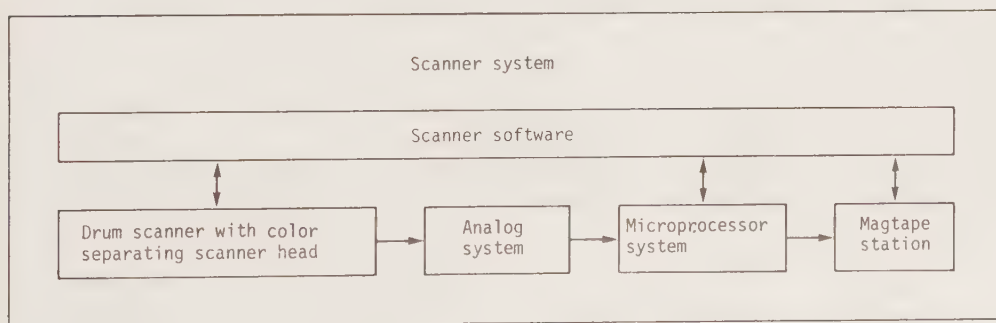


Fig 4-1 The scanner system and its components.

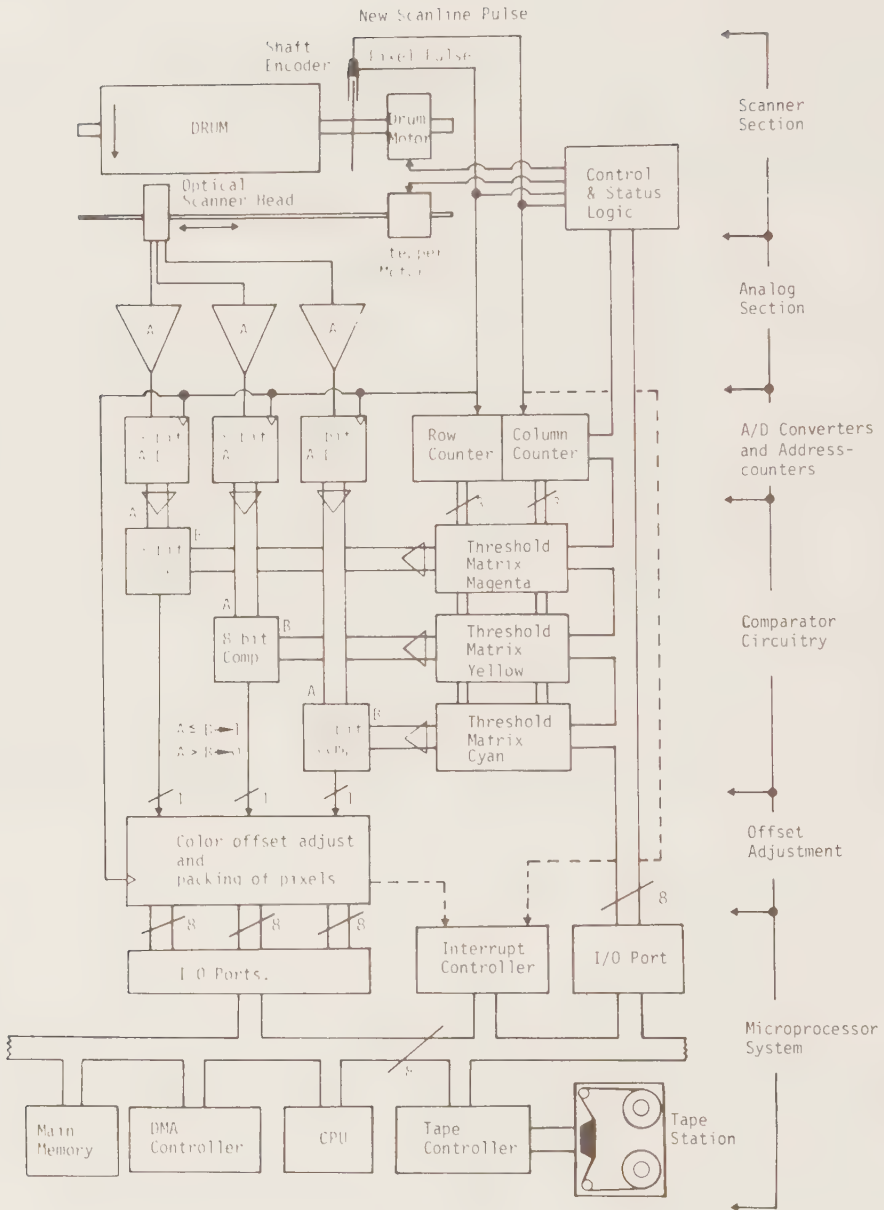


Fig 4-2 Block diagram of the color image scanner.

The analog signal from each of the photodetectors is amplified and A/D converted. This 8-bit digital value is compared in the comparators with a digital threshold value stored in a Dither threshold RWM. After correction for color offset, the result is packed together with 7 other pixel values of the same color to form a byte which is stored in the microprocessor system RWM. When a complete scan line has been stored in the microprocessor system RWM, the entire line is copied through DMA transfers to a magtape station. This is repeated until the entire image is stored on tape. Using this procedure, the image information is compressed 8 times.

During the scanning operation, the shaft encoder delivers information to the drum motor for constant drum surface speed, to the stepper motor for sideways movement of the optical scanner head, to the address counters for addressing the Dither threshold RWMs organized as either four 4 by 4 matrices or one 8 by 8 matrix in each color, to the A/D converter to start conversion of the next pixel, to the color offset adjust for reference when correcting color offset between the colors due to the physical layout of the scanner head and to the packing of pixel circuitry for packing the pixel information into bytes. When a byte is packed, the Programmable Interrupt Controller (PIC) is informed through the dotted line. The PIC directs the microprocessor to retrieve the three bytes, one for each color, and store them in the microprocessor system RWM. The other dotted line to the PIC is activated when the next scan line begins, which initiates the DMA transfer of the previous scan line.

Prior to scanning the three Dither threshold RWMs are loaded from the microprocessor system using the address counters as address latches.

As the stepper motor moves the scanner head sideways, this movement is coupled to the drum rotation, and hence even if the drum surface speed changes during scanner operation, this will have no deteriorating effect on the accuracy of the movement of the scanner head. The drum motor control, stepper motor control and shaft encoder circuitry are described in Bladh (1982).

4.2 Scanner electronics

Most of the scanner electronics is located within the microprocessor system. In the following the microprocessor system with its different interfaces and associated circuitry will be described.

4.2.1 General description of the microprocessor system physical layout

The microprocessor system with its different interfaces is housed in two ordinary 19" racks, as shown in Fig. 4-3. All circuit boards are standard Eurocard size (100 * 160 mm) and all connections between the circuit boards and the backplane bus are made through 96-pole connectors according to DIN 41612. Some of the circuit boards also have connections with the different parts of the scanner system that are outside the microprocessor system. These connections are made through 15, 25 and 50 pole CANNON female connectors mounted in the front panels of these boards.

The backplane bus used in the microprocessor system is an extension of a 96 cavity, 64 pole filled standard bus used within the Department of Electrical Measurements. This "standard" incorporates some signals that are not used in the microprocessor system, such as HOLD and WAITRQ. The "standard" also makes it necessary to alter the read and write signals for memory and I/O. Normally the 8080A microprocessor uses four signals for this, the memory read, memory write, I/O read and I/O write signals. In the present bus four signals are also used, but with another assignment to each signal, namely read, write, memory request and I/O request. In this latter signal assignment two signals must be active to read or write, as opposed to the normal 8080A signal assignment where only one signal is activated for each function.

To avoid problems with overloaded bus signals on the backplane bus, all circuit boards connected to the bus are buffered on their inputs so that they will only draw as much current from the bus as the equivalent of one TTL-load.

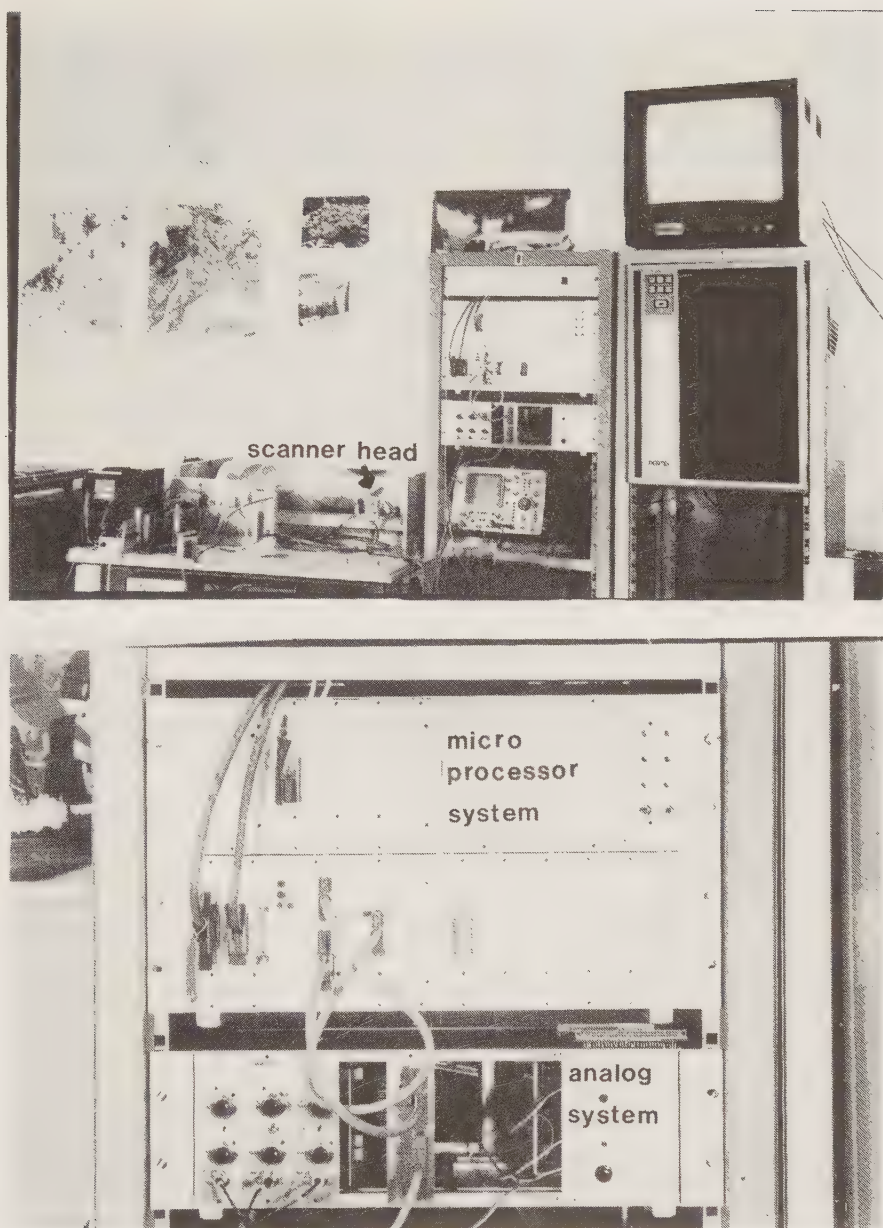


Fig 4-3 Photograph of the image scanner. In the upper half of the figure the entire image scanner system is shown, and in the lower half a closer view of the analog system and the microprocessor system is given.

The backplane bus with its 96 connections is wire wrapped, except for the + 5 V and GND lines. Due to the relatively high current consumption of the system, these lines are made of heavy stranded copper wires, soldered to the bus connectors. This will minimize the voltage drop on these lines.

Each distribution line in the backplane bus is given a name, and this name will be used in the circuit diagrams of the different boards. The pin assignment of the backplane bus is given in Table 4-1.

All the boards in the microprocessor system are shown in Fig. 4-4 together with their connections within the scanner system and some of the essential backplane bus signals.

Each controller and interface of the microprocessor system is not always located on a single circuit board, e.g. the image converter is divided between three different boards. Some boards also contain more than one controller or interface and hence it is not suitable to describe the system board by board. Instead the different controllers and interfaces will be discussed one by one, and their division on different boards will be noticeable only in the complete circuit diagrams added to this report as Appendix A1 through A4.

To make it easier to distinguish between different types of signals present in the circuit diagrams, a coarse division into three different types of signals is made.

- * backplane connections : signals ending in a straight line —
- * front panel connections : signals ending with a triangle —▶
- * signals within a board : signals ending with a filled dot —●

Fig 4-5 depicts different controllers and interfaces that are present in the microprocessor system, and which controls the flow of image information from the analog scanner head to the magtape station.

In the following an attempt is made to describe the hardware involved when transforming a continuous tone image into a bilevel representation and store it on a magnetic tape. The hardware not participating in the actual transfer will be discussed in the latter part of this chapter.

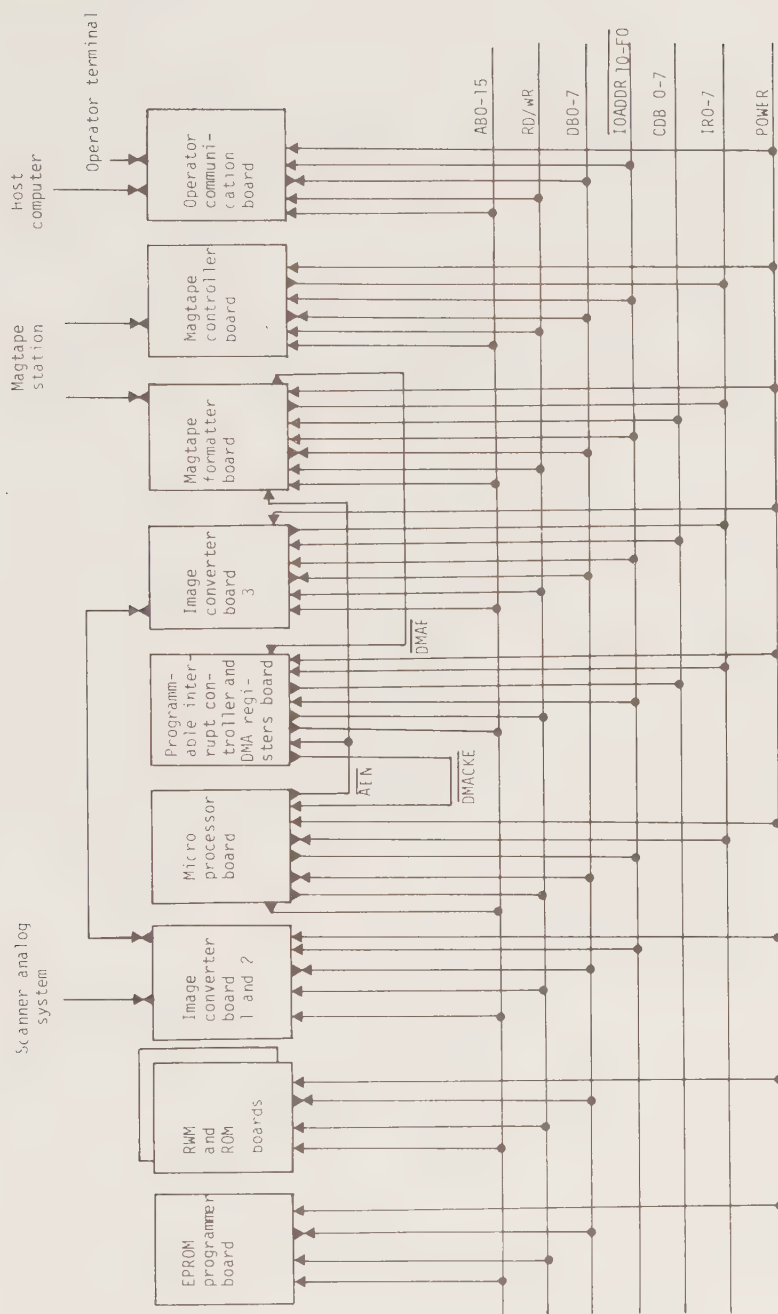


Fig 4-4 The microprocessor system boards, their front panel connections within the scanner system and some essential bus signals.

Pin no.	Row a	Row b	Row c
1	VCC = +5V	VCC = +5V	VCC = +5V
2	$\overline{RD}$	$\overline{DMAE}$	+12V
3	$\overline{WR}$	$\overline{DMAREQ}$	-12V
4	$\overline{MREQ}$	$\overline{AEN}$	+26V
5	$\overline{DHOME}$	$\overline{DMACKE}$	-5V
6	$\overline{WAITRQ}$	$\overline{BCNTRDY}$	AB0
7	$\overline{IORQ}$	$\overline{IOADDR\ 10}$	AB1
8	$\overline{INT}$	$\overline{IOADDR\ 20}$	AB2
9	HOME	$\overline{IOADDR\ 30}$	AB3
10	$\overline{INTA}$	$\overline{IOADDR\ 40}$	AB4
11	$\overline{OUT\ 00} = \overline{IORESET}$	$\overline{IOADDR\ 50}$	AB5
12	$\overline{HOLD}$	$\overline{IOADDR\ 60}$	AB6
13	$\overline{HLDA}$	$\overline{IOADDR\ 70}$	AB7
14	$\overline{DEND}$	$\overline{IOADDR\ 80}$	AB8
15	$\phi XTAL$	$\overline{IOADDR\ 90}$	AB9
16	END	$\overline{IOADDR\ A0}$	AB10
17	$\phi 1TTL$	$\overline{IOADDR\ B0}$	AB11
18	$\phi 2TTL$	$\overline{IOADDR\ C0}$	AB12
19	$\overline{OUT\ 05} = \overline{RESET\ IR5}$	$\overline{OUT\ 0D} = \overline{FSTEP}$	AB13
20	$\overline{OUT\ 06} = \overline{RESET\ IR6}$	$\overline{IOADDR\ E0}$	AB14
21	$\overline{OUT\ 07} = \overline{RESET\ IR7}$	$\overline{IOADDR\ F0}$	AB15
22	$\overline{IR0} = \overline{RTC}$	CDB0	DB0
23	$\overline{IR1} = \overline{HOME/END}$	CDB1	DB1
24	$\overline{IR2} = \overline{PIXELSTROBE}$	CDB2	DB2
25	$\overline{IR3} = \overline{NEXT\ SCANLINE}$	CDB3	DB3
26	$\overline{IR4} = \overline{MAGTAPE\ ERROR}$	CDB4	DB4
27	$\overline{IR5} = \overline{PARITY\ ERROR}$	CDB5	DB5
28	$\overline{IR6} = \overline{GAP\ DETECT}$	CDB6	DB6
29	$\overline{IR7} = \overline{DMA\ DONE}$	CDB7	DB7
30	$\overline{OUT\ 08} = \overline{RESET\ IR1}$	$\overline{OUT\ 03} = \overline{RESET\ IR3}$	$\overline{OUT\ 01} = \overline{START\ DMA}$
31	$\overline{OUT\ 09} = \overline{RESET\ IR1}$	$\overline{OUT\ 04} = \overline{RESET\ IR4}$	$\overline{OUT\ 02} = \overline{RESET\ IR2}$
32	GND	GND	GND

Table 4-1 The Microprocessor system backplane bus pin assignment.

a5	$\overline{\text{DHOME}}$	Signal from HOME position indicator
a9	$\overline{\text{HOME}}$	Inverted and buffred signal from a5
a14	$\overline{\text{DEND}}$	Signal from END position indicator
a16	$\overline{\text{END}}$	Inverted and buffered signal from a14
a19	$\overline{\text{OUT 05}}$	Reset of IR5
a20	$\overline{\text{OUT 06}}$	Reset of IR6
a21	$\overline{\text{OUT 07}}$	Reset of IR7
a22 to		
a29	$\overline{\text{IR 0-7}}$	Interrupt request signals to the PIC
a30	$\overline{\text{OUT 08}}$	Reset of IR1 when in END position
a31	$\overline{\text{OUT 09}}$	Reset of IR1 when in HOME position
b2	$\overline{\text{DMAE}}$	DMA enable
b3	$\overline{\text{DMAREQ}}$	DMA request
b4	$\overline{\text{AEN}}$	DMA address enable
b5	$\overline{\text{DMACKE}}$	DMA clock enable
b6	$\overline{\text{BCNTRDY}}$	Bytecount ready, DMA transfers completed.
b7 to	$\overline{\text{IOADDR}}$	
b21	$\overline{\text{IO-F0}}$	Predecoded address lines for I/O
except		
b19	$\overline{\text{OUT 0D}}$	Force stepper motor to start
b22 to		
b29	$\overline{\text{CDB 0-7}}$	Control data bus
b30	$\overline{\text{OUT 03}}$	Reset of IR3
b31	$\overline{\text{OUT 04}}$	Reset of IR4
c6 to		
c21	$\overline{\text{AB 0-15}}$	Address bus 0-15
c22 to		
c29	$\overline{\text{DB 0-7}}$	Data bus 0-7
c30	$\overline{\text{OUT 01}}$	Start a new block of DMA transfers
c31	$\overline{\text{OUT 02}}$	Reset IR2

Table 4-1 cont. Short description of some of the signals on the backplane bus.

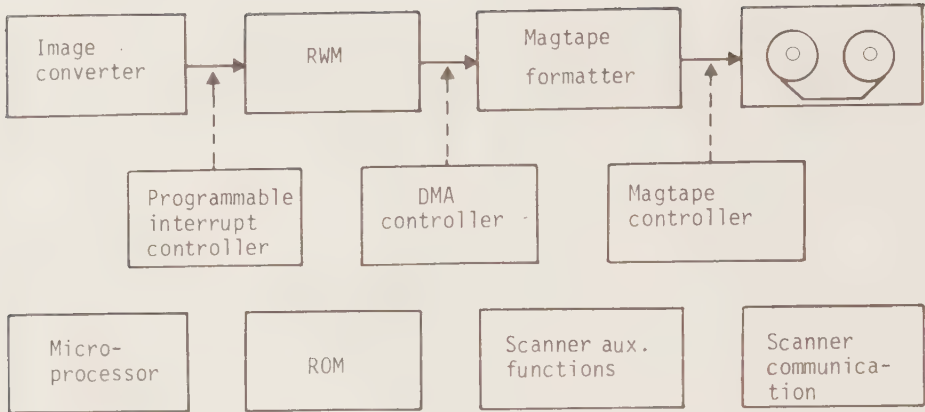


Fig 4-5 The main blocks of the microprocessor system including the magtape station. Level A converts the image information and transfers it through the micro-processor system onto the magtape. Level B controls these functions and level C provides the utilities necessary for level A and B to operate.

4.2.2 The Image converter

The image converter receives the analog image information from the analog circuitry which is located between the scanner head and the microprocessor system as shown in Fig. 4-1. It transforms the analog information into a stream of digital image information using a Dither threshold technique described in Nilsson and Nygren (1981B). Thereafter it passes the digital image information over to the micro-processor.

A block diagram of the image converter is given in Fig. 4-6. The image converter is actually located on three different boards in the micro-processor system. The circuit diagrams of these boards and the front panel connectors pin assignment are given in Appendix A1.1-12.

When the analog information is A/D converted into digital values, only samples of the information is converted. As the resolution of the scanner must be 0.2 mm, at least two samples must be taken in this interval to fulfill the sampling theorem. The sampling theorem states that the sampling frequency must be at least twice as high as the sampled frequency if one can assume that the curve form of the sampled frequency is sinusoidal.

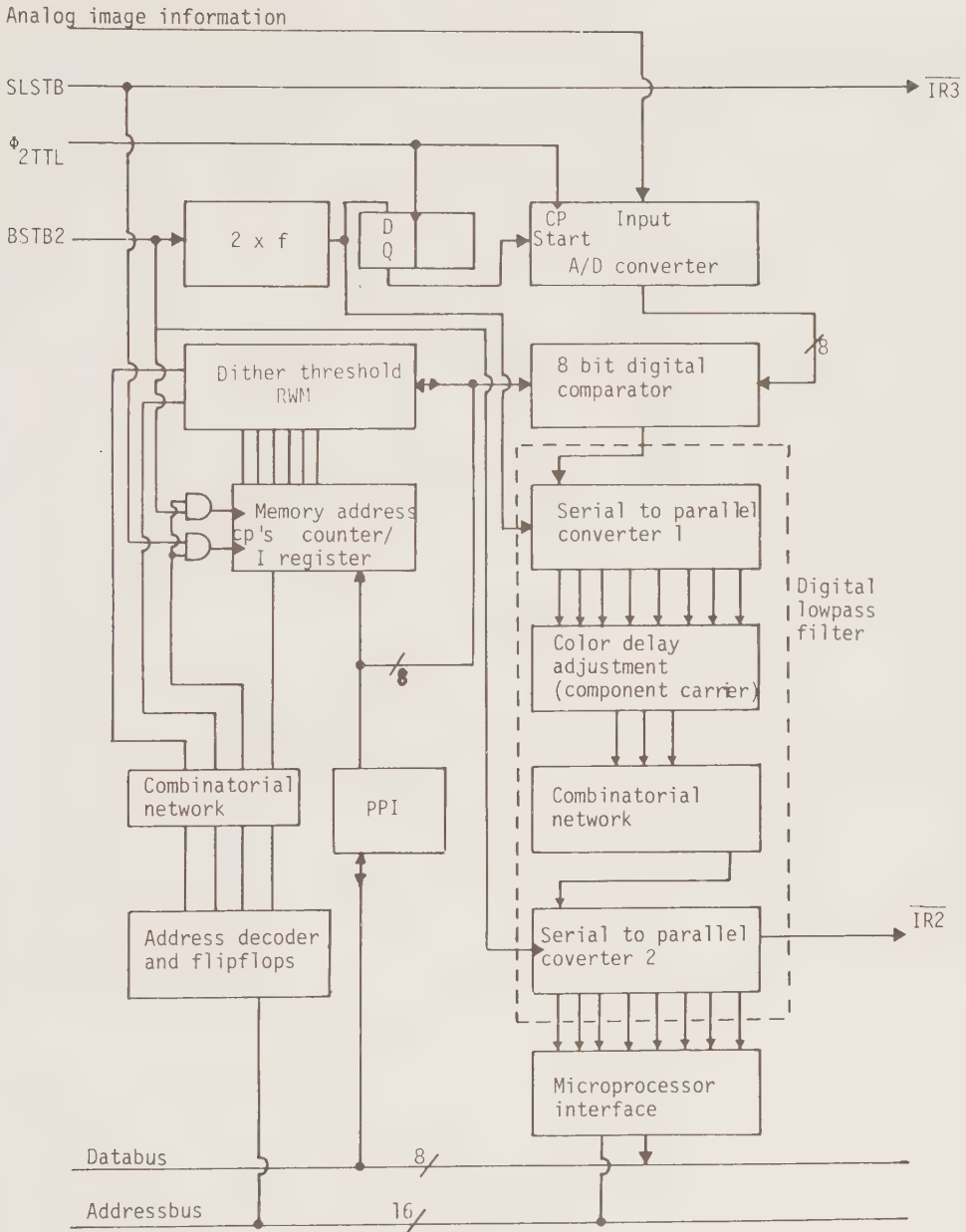


Fig 4-6 Block diagram of the image converter. Only the magenta channel is shown as it's PPI port is also used to address the Dither threshold RWMs.

To be able to take these samples at the correct time intervals independent of drum rotation speed, the signal BSTB2 (Bit strobe 0.2 mm) is used as a reference signal. BSTB2 originates from the shaft encoder on the drum motor axis. It delivers 3360 pulses for each complete revolution of the drum. This corresponds to 1 pulse/0.2 mm movement of the drum surface.

To manage two A/D conversions while the drum surface moves 0.2 mm, the BSTB2 signal must be frequency doubled to deliver 1 pulse/0.1 mm. This is achieved in the frequency doubling network where each edge of the square wave BSTB2 is transformed into a pulse.

Before this pulse, called BSTB1 (Bit strobe 0.1 mm) can be used to start the A/D conversions it is synchronized with the A/D converter clock. The reason for this is that the manufacturer of the A/D converter states in the specifications that the converter requires the startsignal to be low at least 50 ns prior to the rising edge of the clock to function properly. The best way to assure this is to synchronize the start signal with the clock signal.

The digital values from the A/D converter are compared to Dither matrix threshold values in an 8 bit digital comparator. The matrix threshold values are produced by the local RWMs where they are deposited before starting a scanning operation as described below. They are altered after each 0.2 mm movement of the drum, as the BSTB2 signal clocks the address counter/register. Thus two comparisons are made with each threshold value. The result of each comparison is either a "1" or a "0". This bit is shifted into the Serial to Parallel converter 1 (S/P1).

At this point in the image converter circuit, each 0.2 mm pixel on the drum surface is represented by two bits. Since only one bit is required for each pixel, this must be reduced to one bit before the image information leaves the converter.

The reduction is achieved in hardware using a digital lowpass filter. The filter consists of two serial to parallel converters, S/P1 and S/P2 which use different clock frequencies and a combinatorial network located between them. Also, a color delay circuit is included here which will be described below. The three last bits from the comparator, representing 0.3 mm drum surface, are presented to the combinatorial network in parallel by the S/P1. The network determines according to Table 4-2 which logical level is in majority among these and passes this level onto its output.

Pixels with 0.1 mm diameter			Majority logic output
N-1	N	N+1	
=====			
0	0	0	0
0	0	1	0
0	1	0	0
0	1	1	1
1	0	0	0
1	0	1	1
1	1	0	1
1	1	1	1

Table 4-2 The algorithm used to reduce the noise in images generated by image information with line densities greater than 5 lines/mm

S/P2 is clocked at half the frequency of the S/P1, and hence only every other bit from the combinatorial network is shifted into the S/P2. This results in one bit/0.2 mm pixel. The advantage of this method compared to making only one sample in each 0.2 mm pixel is that this bit is based on three consecutive 0.1 mm samples.

When 8 bits are entered into the S/P2, the PIC (Programmable Interrupt Controller) is activated through the IR2 interrupt request line. The microprocessor is then directed to retrieve the three bytes, one for each of the colors, from the image converter through three PPI ports A, B, and C, one for each color.

One further correction different for each color must be made in the converter. Due to the physical layout of the optical scanner head the three photodetectors do not view the same pixel simultaneously (Nilsson 1981). Hence the information reaching the A/D converters at any given time is coming from different but adjacent pixels. Thus a constant phase shift exists between the three color signals. By delaying the information from the cyan detector one BSTB1 pulse, and the information from the yellow detector two BSTB1 pulses, all three colors (magenta, cyan and yellow) this phase shift can be eliminated. This delay is introduced in the digital lowpass filter by connecting three consecutive outputs of the S/P1 to the three inputs of the combinatorial network using a component carrier which can be altered easily.

Prior to the operation of the image converter, the Dither matrix threshold RWMs must be loaded from the microprocessor with the threshold values. As shown in Fig 4-6, for this purpose four signals, are encoded as I/O addresses, and as each signal can be set in two states, 8 I/O addresses are used. The signals are:

	instruction mnemonics
=====	
DRLC = Dither RWM Load Cycle disable	OUT A8
$\overline{\text{DRLC}}$ = Dither RWM Load Cycle enable	OUT A9
DRAL = Dither RWM Address Load disable	OUT AA
$\overline{\text{DRAL}}$ = Dither RWM Address Load enable	OUT AB
DRR/W = Dither RWM Read	OUT AC
$\overline{\text{DRR/W}}$ = Dither RWM Write	OUT AD
DRDC = Dither RWM Data Check disable	OUT AE
$\overline{\text{DRDC}}$ = Dither RWM Data Check enable	OUT AF

To avoid the possibility of conflicting settings of these signals, a combinatorial network is added. It avoids situations such as a Dither RWM Data Check enable while the Dither RWM Load Cycle is disabled.

The loading of the Dither threshold RWM can be described like this:

The signal $\overline{\text{DRLC}}$ is activated by the microprocessor, and the counter/register will stop any counting of pulses on the SLSTB (next Scan Line strobe) and BSTB2 (Bit strobe 0.2 mm) lines. Then the microprocessor sends the first address byte to the PPI, port A. These 8 bits allow to address up to 256 memory cells, thus matrices as large as 16 by 16 threshold values may be used. However in the present case only 64 memory cell are necessary in the RWM, and thus only the 6 least significant bits of this byte are needed to define the address. The address is loaded into the counter/register by activating the signals DRAL, $\overline{\text{DRAL}}$ and DRAL again. This generates a pulse which clocks the address into the counter/register. An instant later this address reaches the three RWMs, and the memories are now ready to accept threshold information from the microprocessor for this particular address. The microprocessor sends this 3 * 8 bit threshold information to the port A, B and C of the PPI. From here the information is loaded into the RWMs by activating the signals DRR/W, $\overline{\text{DRR/W}}$ and DRR/W again, which generates a write strobe to the memories. This ends the loading sequence of three memory cells, one for each of the colors. The entire procedure is repeated until all 64 memory cells in each of the three colors are loaded.

With all memory cells loaded, the contents of each cell is read back into the microprocessor for verification. The procedure resembles the loading procedure described above but now the threshold values are moved in the opposite direction. To enable the outputs of the RWMs the $\overline{\text{DRDC}}$ -signal must be activated and all three ports in the PPI must be reprogrammed as input ports. Prior to each verification of a Dither threshold RWM cell, the address to this cell must be given to the counter/register. Therefore the PPI port A must be reprogrammed to output mode and the DRDC signal activated between every transfer.

If this verification is without errors, the PPI ports are all set in input mode and the DRDC signal is activated. A scanner operation can start.

The detailed circuit diagram is given in Appendix A1.1-1.10, which show the layout of three circuit boards. Here the A/D converter and the comparator circuitry are located on board I, the Dither RWM with control and loading circuitry on board II, and the lowpass filter is divided between board I and III.

4.2.3 The programmable interrupt controller (PIC)

The PIC controls the transfer of image information from the image converter S/P2 to the microprocessor system RWM. It also handles several other tasks which are described in chapter 3.4.

The D flipflops added to all interrupt request lines except IRO, are used to externally prevent an interrupt request from reaching the PIC. Each flipflop is set the first time an interrupt request occur on the interrupt request line. As the PIC responds to positive going edges all further interrupt requests on the same line will be ignored until one of the OUT instruction (02-09) is issued by the microprocessor via the address predecoder (c.f. chapter 4.2.8) and the flipflop is cleared. This instruction is normally issued at the end of each interrupt service routine for the interrupt request line in question.

The PIC is physically located on the same board as the DMA controller registers and counters. The circuit diagram is given in Appendix A2.2. In Fig 4-7 a block diagram of the programmable interrupt controller is shown.

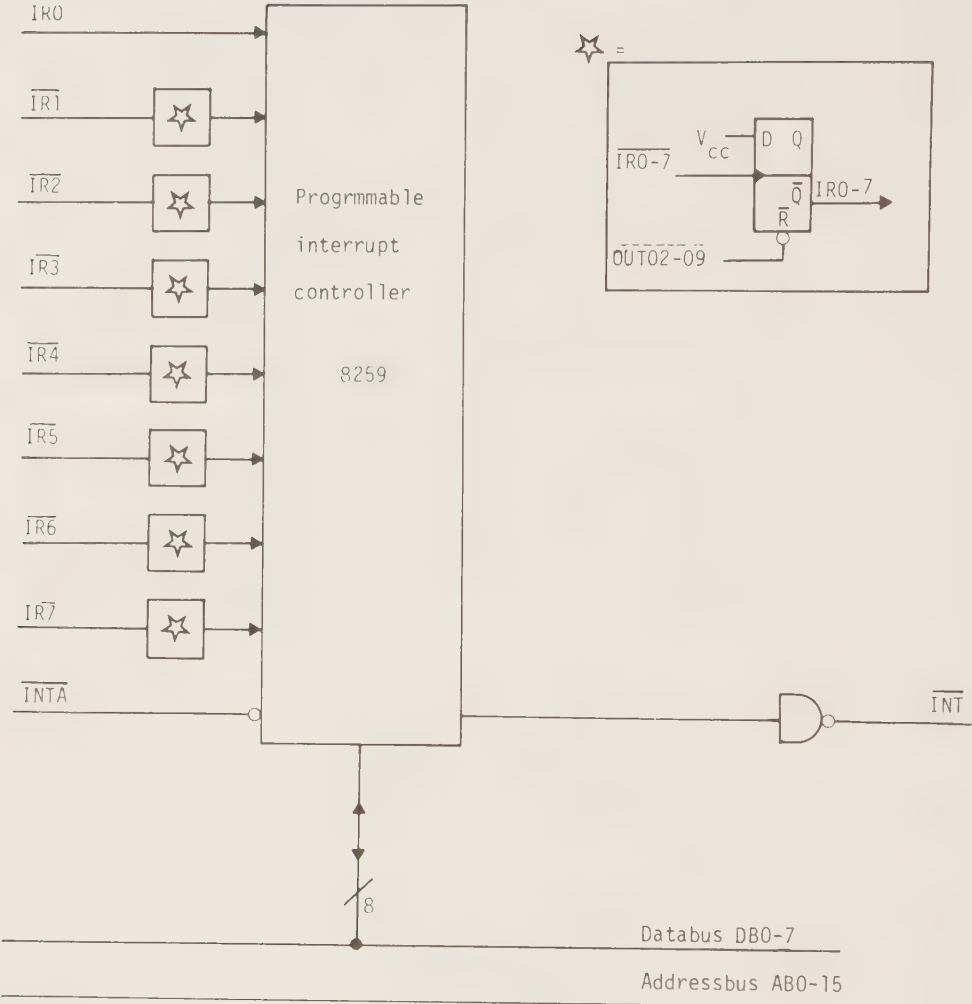


Fig 4-7 Block diagram of the programmable interrupt controller's external connections.

4.2.4 The microprocessor System RWM

The image information from the image converter S/P2 is stored in the microprocessor system RWM, as described in chapter 3.4.2. All microprocessor RWM's and ROM's are located on special memory boards which will be described in this chapter.

This general memory board is shown in Fig 4-8 and its component layout in Fig. 4-9. It is designed with flexibility in mind. Hence either RWM or ROM chips can be installed on this board. When being used as a RWM board, 1 kbyte static RWM chips (4118), are used. Thus the board can contain up to 8 kbytes of RWM.

To use the board for RWMs require some initial preparations which are different from the preparations necessary when the board is used for ROMs. These initial preparations for a RWM board will be described in the following.

The 74138, 3 to 8 decoder, is inserted in the socket marked B, as shown in both Fig. 4-8 and 4-9. The decoder resolves the address from the bus in increments of 1 kbyte within the boundaries set by the 7485 4 bit comparator. The comparator selects the 8 kbyte address range assigned to this board.

The 16 pin component carrier (CC) with the pins 4, 7, 9, 10, 11, 12, 13, 14 and 15 interconnected is inserted in the socket marked A and thereby provides the memory chips with the $\overline{RD}$ signal.

The dip switches S5 and S6 are closed, while the dip switches S7 and S8 are open. S5 disables the latching function in the memory chips for the address and chip select ($\overline{CS}$) lines, normally used in microprocessor systems with a common multiplexed address and data bus, and S6 enables the $\overline{WR}$ -signal to all eight chips on the board. Dip switches S7 and S8 must be open if S5 and S6 are closed and vice versa.

The board is now ready to accept RWM chips. Before it is inserted in the microprocessor system, an 8 kbyte address range must be chosen, and the addressing mode selected. Dip switches S1, S2 and S3 are used for setting the start address of the board, as shown in Table 4-3. Dip switch S4 is used for the addressing mode selection. In this microprocessor system the signal $\overline{MREQ}$ is used as described in chapter 4.2.1. Hence the $\overline{MREQ}$ signal cannot be connected to GND and therefore the dip switch S4 is open.

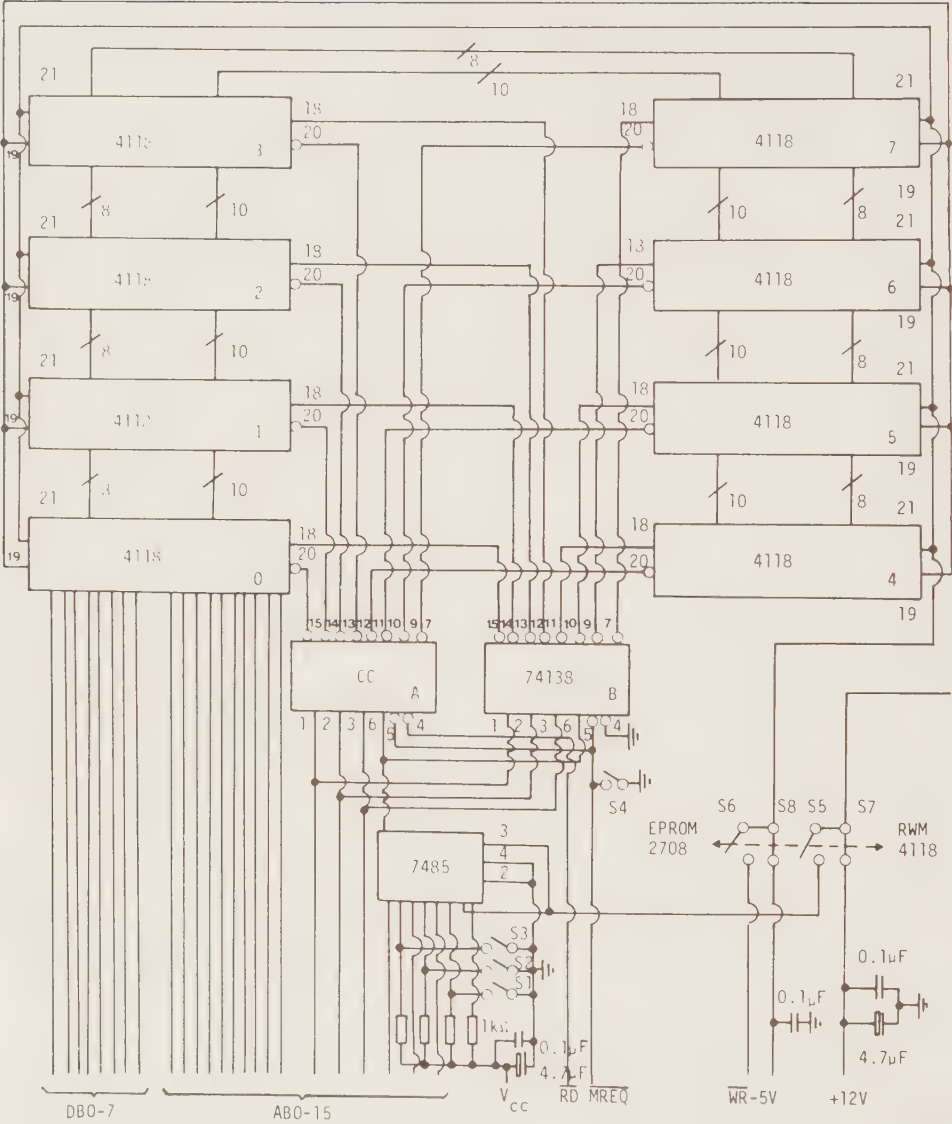


Fig 4-8 The microprocessor system RWM circuit diagram.

Frontpanel

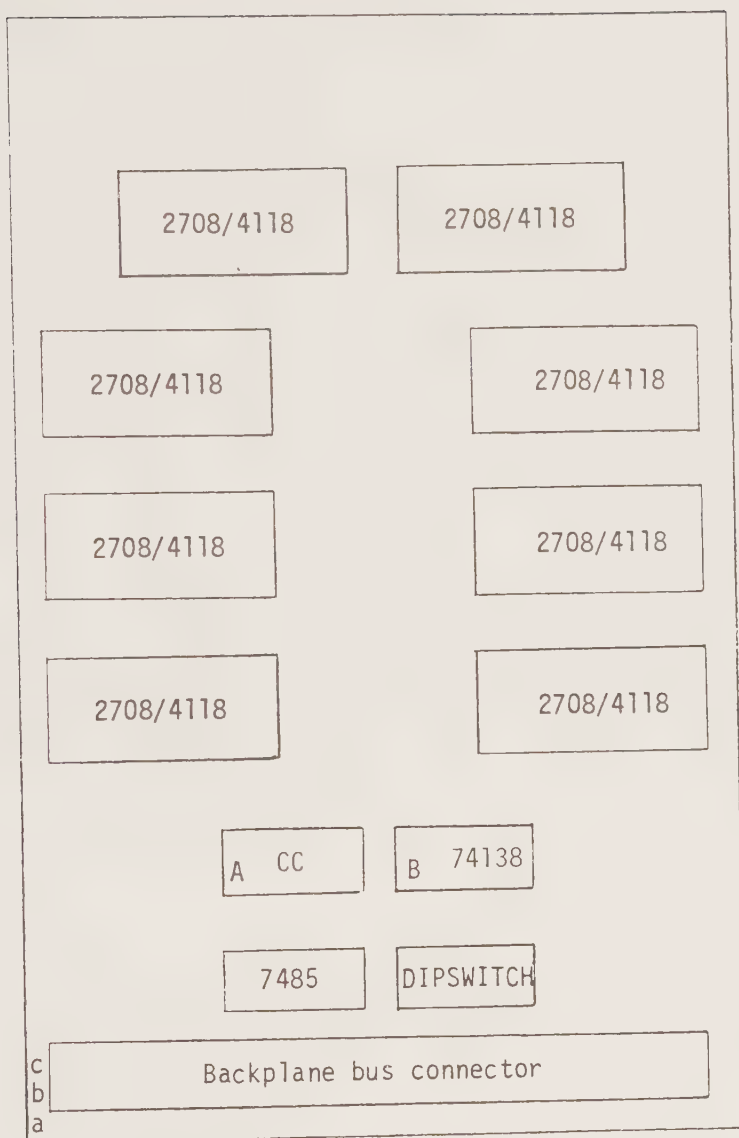


Fig 4-9 The microprocessor system RWM board component layout.
Board seen from component side.

Dip switch			Start address of memory board in hexadecimal notation
S1	S2	S3	
=====			
closed	closed	closed	0
"	"	open	2000
"	open	closed	4000
"	"	open	6000
open	closed	closed	8000
"	"	open	A000
"	open	closed	C000
"	"	open	E000

Table 4-3 Start address selection for memory boards.

The 8 kbyte of RWM on a board is more than enough for the needs of the scanner system. Beside the two 1296 bytes long scan line buffers, only a few memory cells for the microprocessor stack and some variables that changes during program execution are necessary. As the present microprocessor system was used for developing its own software, this prototype microprocessor system actually contains 16 kbytes of RWM located on two boards.

4.2.5 The Transparent DMA Controller

The transparent DMA controller moves the image information from the microprocessor system RWM to the magtape formatter. The controller is started when the image information of one scan line is deposited in the microprocessor system RWM. The transfer has to be completed before the next scan line is stored in the RWM and ready to be transferred.

A block diagram of the transparent DMA controller is shown in Fig. 4-10 (Nygren et al., 1980). The controller consists of:

- * a DMA controller logic, which monitors the processor activity and determines when the busses are free to use for DMA transfers.
- * a start address register, which holds the microprocessor system RWM address of the first byte to be transferred in the DMA transfers.

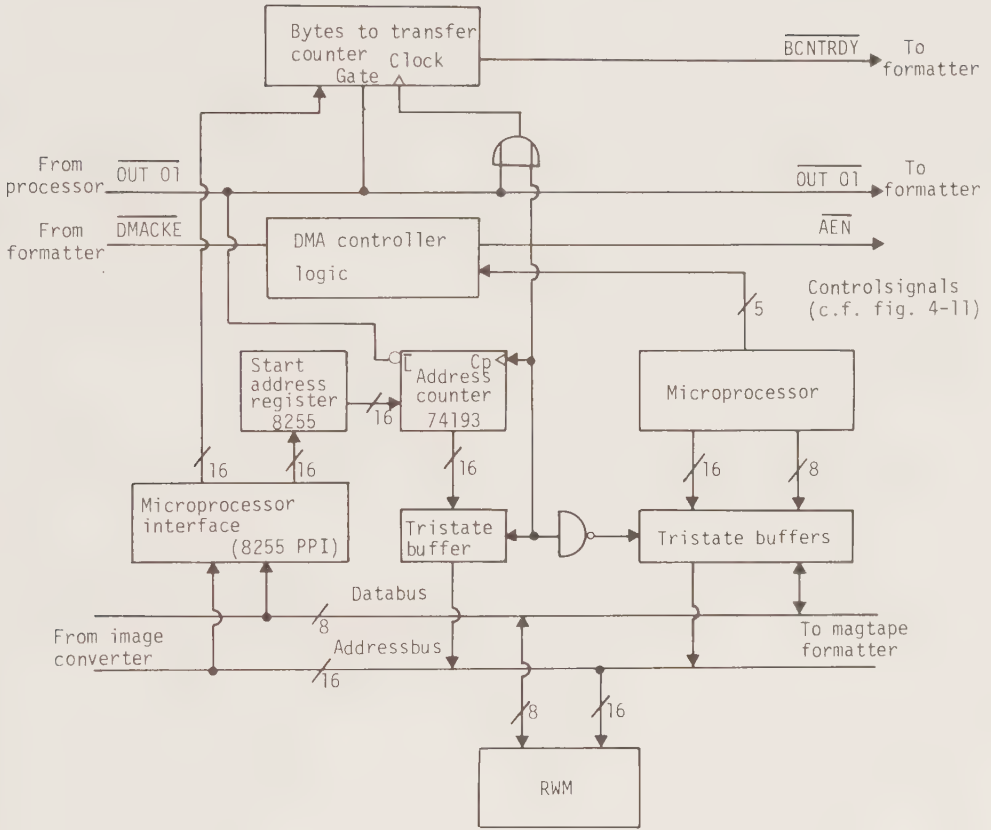


Fig 4-10 Block diagram of transparent DMA controller.

- * an address counter, which is loaded from the start address register prior to the first DMA transfer. The counter is used as the memory address pointer in all DMA transfers and it is incremented for each successive DMA transfer by the $\overline{\text{AEN}}$ signal.
- * a bytes to transfer counter, which holds the number of bytes to transfer in the next block of DMA transfers. It is loaded once and for all prior to the first block of DMA transfers. For each DMA transfer of a byte, its contents is decremented by 1. When the terminal count is reached (counter=0) the counter outputs the signal $\overline{\text{BCNTRDY}}$ (Byte CouNT ReaDY). The counter is internally reloaded with the number of bytes to transfer when receiving the start pulse ($\overline{\text{OUT01}}$) of the next block.

Before a detailed description of the DMA controller logic and a single DMA transfer is presented, a short summary of the sequence in a complete block of DMA transfers will be given.

- * The microprocessor loads the start address register and the bytes to transfer counter according to the description given above.
- * The microprocessor issues the OUT 01-instruction. This instruction generates the start pulse for the DMA controller via an address decoder (c.f. chapter 4.2.8) This decoded start pulse is given the same name as the instruction, $\overline{\text{OUT01}}$.
- * The start pulse, $\overline{\text{OUT01}}$,
 - loads the address counter with the contents of the start address register
 - loads the bytes to transfer counter with the appropriate preset value.
 - decrements the bytes to transfer counter by 1
 - initiates the first DMA request through the magtape formatter board, which results in $\overline{\text{DMACKE}}$ going active.

As soon as the DMA controller logic detects that the microprocessor is not using the busses (which always occur within 2 microseconds), it activates the $\overline{\text{AEN}}$ -signal.

The $\overline{\text{AEN}}$ -signal disables the microprocessors data and address bus connections, and enables the DMA controller address counter. Within 500 ns the first byte is transferred from the microprocessor RWM to the magtape formatter data buffer register, and the bytes to transfer counter is decremented by 1.

As soon as the magtape formatter has moved the byte from its data buffer it requests a new DMA transfer. This results in $\overline{\text{DMACK}}\text{E}$ going active and the latter part of the description above is repeated. When the last byte is transferred, the $\overline{\text{BCNTRDY}}$ signal will inform the magtape formatter that all bytes are transferred.

The main difference between the transparent DMA controller and commercially available units is the effect the DMA transfers have on the microprocessor normal program execution. While the commercial units halts the processor during a transfer, the transparent DMA controller makes the transfers without affecting the normal processor activity.

In Fig 4-11 the entire controller logic is shown. In the following the timing of a DMA transfer will be discussed:

The two JK flipflops in the middle of the circuit diagram generates the signal DMAOK as shown in the timing diagram given in Fig. 4-12. This signal is active in all states that allow DMA transfers, i.e. in all states except 2 and 3. If the signal DMAOK is active and a DMA request is made through the $\overline{\text{DMACK}}\text{E}$ signal, nothing will happens until the first free state is encountered. This is assured by using the two clocks, $\phi_{1\text{TTL}}$ and $\phi_{2\text{TTL}}$. The reason for this delay which will occur even in free states, is that the DMA transfer requires a complete state to make the transfer. In the timing diagram given in Fig. 4-12 three different examples of DMA requests are given. First a DMA transfer is successful in state 1, then a DMA request is pending in state 3. As no DMA transfers can be carried out in this state, this transfer is made in state 4. Finally a DMA request is made too late in state 5, and hence will not be serviced until next state. Thus during this machine cycle two DMA transfers have been made.

Although the DMA controller operates without errors in this design, an additional modification was made as the timing diagram indicates a possible error if the normal $\overline{\text{WR}}$ signal is used. The possible error might occur if a DMA request is pending in state 3, and the processor is writing information to the memory. At the beginning of state 4 both the address and the $\overline{\text{WR}}$ signal will be removed simultaneously and there is a probability that erroneous writes might occur in other memory addresses because of this. To avoid this flaw in the timing diagram, the normal $\overline{\text{WR}}$ -signal is replaced by the $\overline{\text{WRITE}}$ -signal which is clocked on the $\phi_{2\text{TTL}}$ clocks falling edge as shown in Fig 4-12.

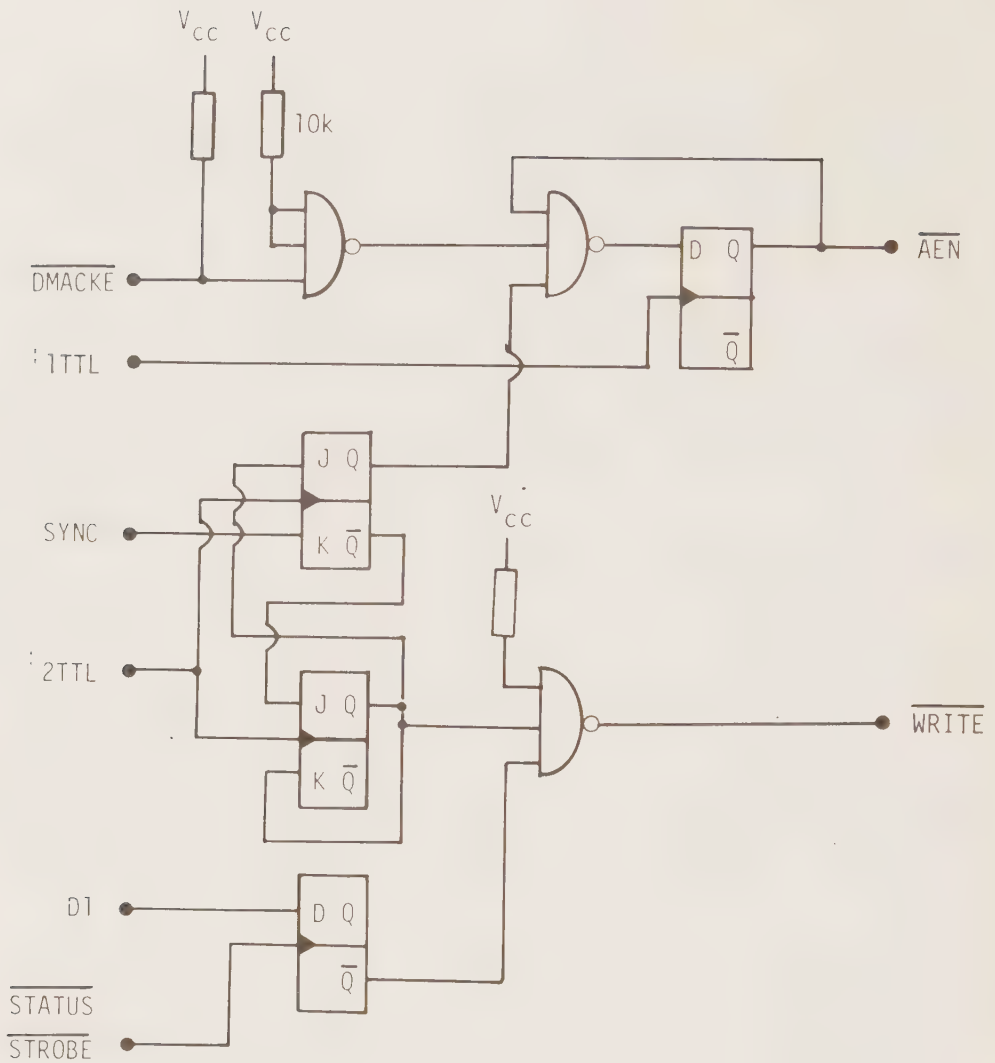


Fig 4-11 The transparent DMA controller logic circuit diagram. When a DMA request is pending, $\overline{\text{DMACKE}}$ will go active. On the first free 500 ns state, the signal $\overline{\text{AEN}}$ will "disconnect" the microprocessor from the address and data busses and start a DMA transfer.

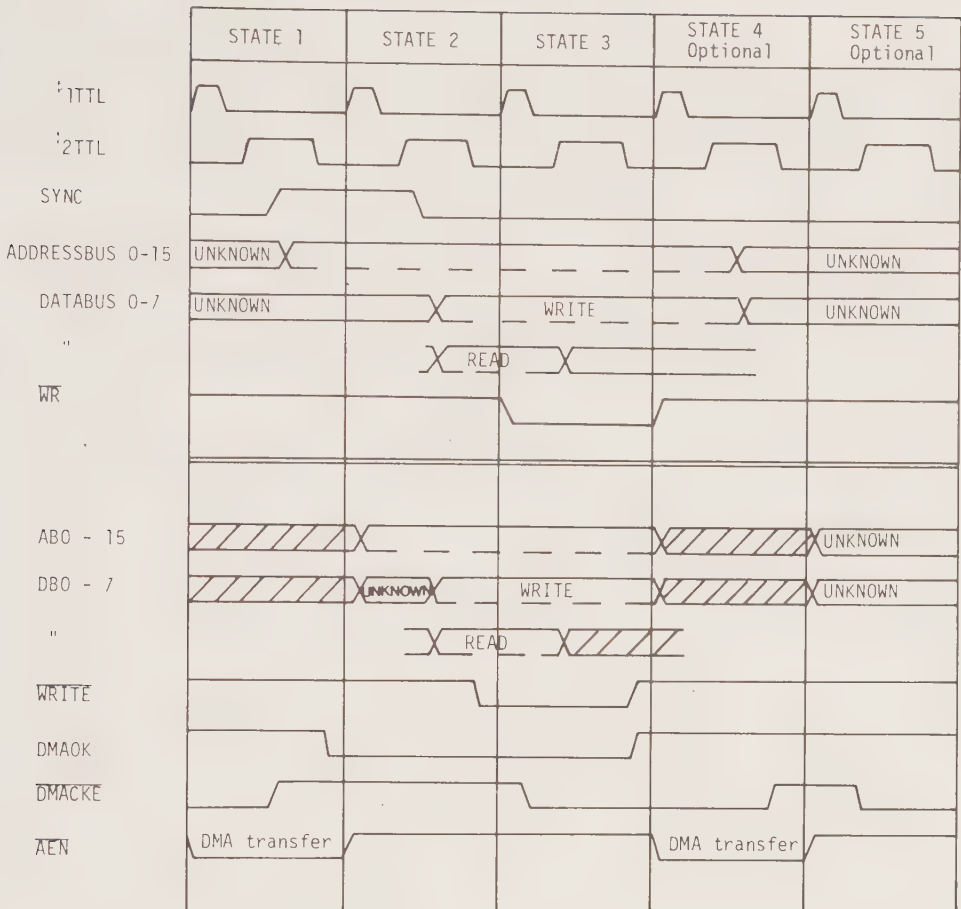


Fig 4-12 Timing diagram of the 8080A microprocessor. The normal timing is shown in the upper part of the diagram. The alterations due to the transparent DMA controller are given in the lower part of the diagram. The asynchronous signal $\overline{DMACKE}$, which indicates a DMA transfer request, is arbitrary chosen.

The transparent DMA controller is physically divided into two parts located on different boards. The DMA controller logic is placed on the microprocessor board, while the DMA registers and counters are located on the same board as the programmable interrupt controller. A complete circuit diagram is given in Appendix A2.2-3 and A4.2.

4.2.6 The Magtape formatter

The reason for developing a tape formatter was the high cost of commercially available units. Today this cost has dropped considerably and hence this formatter is not used in new designs.

The tape formatter is the link between the microprocessor system and the magnetic tape station with its electronic circuitry. Its main functions in the scanner system are:

- a) start tape movement by activating the SFC signal (Synchronous Forward Control)
- b) wait for the tape to reach its nominal speed (Start delay)
- c) request data from DMA controller and write it onto the tape at a constant rate.
- d) when the last data byte is written on the tape, as indicated by the signal BCNTRDY, the formatter should add the CRCC (Cyclic Redundancy Check Character) and the LRCC (Longitudinal Redundancy Check Character) to the record
- e) add a short delay (stop write delay)
- f) stop tape movement by deactivating the SFC signal
- g) wait for tape motion to stop (stop delay)
- h) activate $\overline{\text{IR7}}$, DMA transfer completed interrupt request

To perform these different functions a complicated electronic circuitry is required. Therefore it is difficult to give an easily understandable description at the component level. Hence this board will be described with the block diagram shown in Fig. 4-13 as reference. For a more detailed study of the electronic circuitry, the formatter circuit diagrams and front panel connector pin assignment are included in Appendix A3.1-5

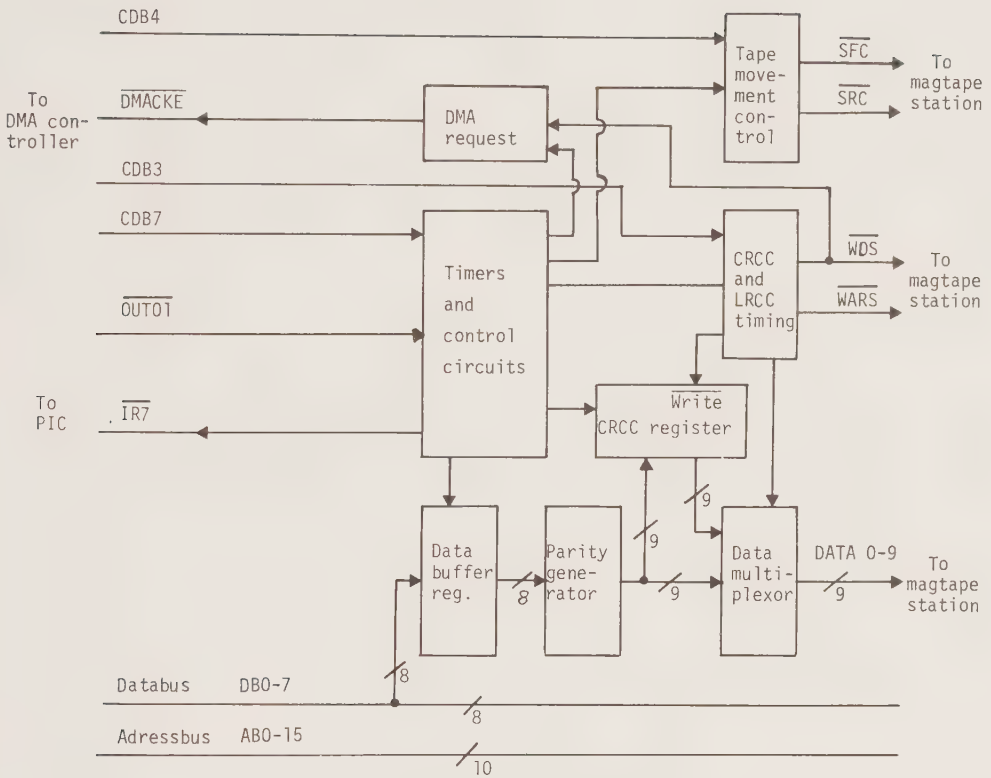


Fig 4-13 Block diagram of the magtape formatter.

In the following the magtape formatter operation will be described in more detail.

Prior to the operation of the magtape formatter, the initiation routine described in chapter 3.3.5 is carried out. Five signals that can be altered during operation are also set, namely:

- CDB3 : length of write strobe to the magtape station (1 μ s or 2 μ s)
- CDB4 : direction of magtape movement (reverse/forward)
- CDB5 : WARS (Write Amplifier Reset Strobe) (disable/enable)
Enables the output of LRCC at the end of a record.
- CDB6 : Cyclic Redundancy Check Character on tape (disable/enable)
- CDB7 : DMA transfer direction (Magtape write/read) (output/input)

When the magtape formatter receives the $\overline{\text{OUT01}}$ signal, it starts the tape movement by activating the SFC (Synchronous Forward Command) signal. As it takes some time for the magtape station to accelerate the tape to its nominal speed, a start tape delay is added (18 ms for the 37.5 ips magtape station). During this delay the first byte is transferred by the DMA controller from the microprocessor system RWM to the magtape formatter data buffer register. When the delay expires, the first byte is written onto the tape with the WDS (Write Data Strobe) signal. The WDS signal immediately generates a new DMA request $\overline{\text{DMACKE}}$ to the DMA controller, and within a few microseconds the next byte is placed in the data buffer register.

Before the data from the buffer is written on the tape, a parity bit is added in the parity generator and thus 9 parallel bits are written on the tape. All image information sent to the magtape station is also read by the CRCC register. This is necessary as the CRCC register must be able to generate the CRCC information that is added at the end of each record on tape.

When all 1296 bytes have been transferred to the magtape, the LRCC and CRCC information is written onto the tape. Thereafter a short write stop delay is added before the signal SFC is deactivated (3 ms for the 37.5 ips magtape station). As it takes some time for the tape to stop its motion, a stop tape delay is added (12 ms for the 37.5 ips magtape station).

When the tape is stopped the magtape formatter issues the DMA transfer completed interrupt request, $\overline{\text{IR7}}$ (c.f. chapter 3.4.4).

4.2.7 The Magtape Controller

The controlling and the supervising functions for the magtape station are located on a single board. This board, shown in Fig. 4-14 and 4-15, with component layout as in Fig. 4-16, was first designed for the magtape station only, and later an extra 8255 PPI I/O port was added for connection to a line printer during software development

The I/O ports are based on the 8255 PPI (Programmable Peripheral Interface) with three 8-bit bidirectional ports. The data direction in each port is programmed from the microprocessor, and the control and status lines, going to/from the magtape station are buffered for higher noise immunity.

The use of the three ports A, B, and C of the 8255A PPI is the following:

Port A is an 8 bit output port for magtape station
control

PA0 SeLecT magtape unit, select bit 0	SLT0
PA1 Data Density Select 800/1600 bpi	DDS
PA2 OVerWrite	OVW
PA3 Load On Line	LOL
PA4 Set Write Status	SWS
PA5 Read ThresHold	RTH
PA6 OFF line Command	OFFC
PA7 SeLecT magtape unit, select bit 1	SLT1

Port B is an 8 bit input port for status information on
magtape station and scanner head position.

PB0 magtape station ReaDY	RDY
PB1 High DensIty (1600 bpi)	HDI
PB2 File write ProTect	FPT
PB3 Write ENable	WEN
PB4 at Load Point	LDP
PB5 ReWinDing	RWD
PB6 scanner head at HOME position	HOME
PB7 scanner head at END position	END

Port C is a 4 bit output (PC0-PC3) and 4 bit input (PC4-PC7) port. All 8 bit are used for magtape control and status.

PC0 select magtape unit, select bit 2	SLT2
PC1 Synchronous Forward Command	SFC
PC2 Synchronous Reverse Command	SRC
PC3 ReWind Command	RWC
PC4 GAP DETect	GAPDET
PC5 RuNninG	RNG
PC6 End Of Tape	EOT
PC7 ONLine	ONL

To enable error detection in the magtape station operation, three signals PC5-PC7 can generate an interrupt on level 4 (IR4). The interrupt service routine will read the three bits at the C port to determine which one of them caused the interrupt request, and thereafter initiates the appropriate program in the microprocessor.

All signals going out from the PPI are static, except signal PC3. This output bit starts the rewinding of the tape and is only a short pulse. Therefore a monostable flip-flop is used which generates a predefined pulse independent of the length of the signal coming from the PPI PC3 port.

Two input signals, PB6 and PB7 are not connected to the magtape station. Instead they indicate the status of the HOME and END position microswitches. Their use in the system will be described in chapter 4.2.8.

The connections in the 25 pole female CANNON connector marked P on the front panel of the magtape control and status board are given in Table 4-8. The additional PPI located on this board is unbuffered, so that all ports can be used for input or output at will. Its 25 pole female CANNON connector located on the same front panel is marked X. The connections are given in Table 4-9.

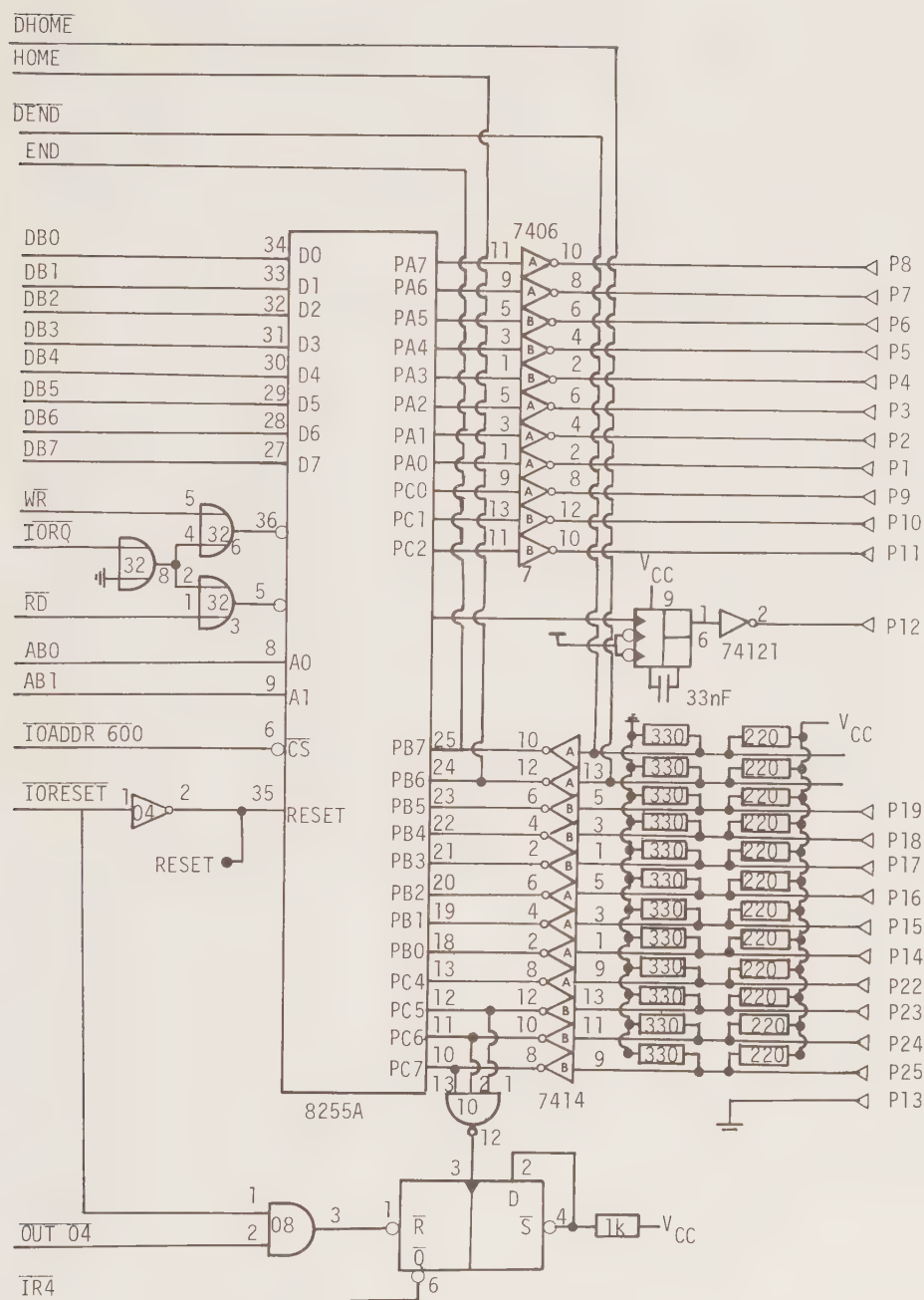


Fig 4-14 The magtape control and status board circuit diagram 1, the magtape control and status.

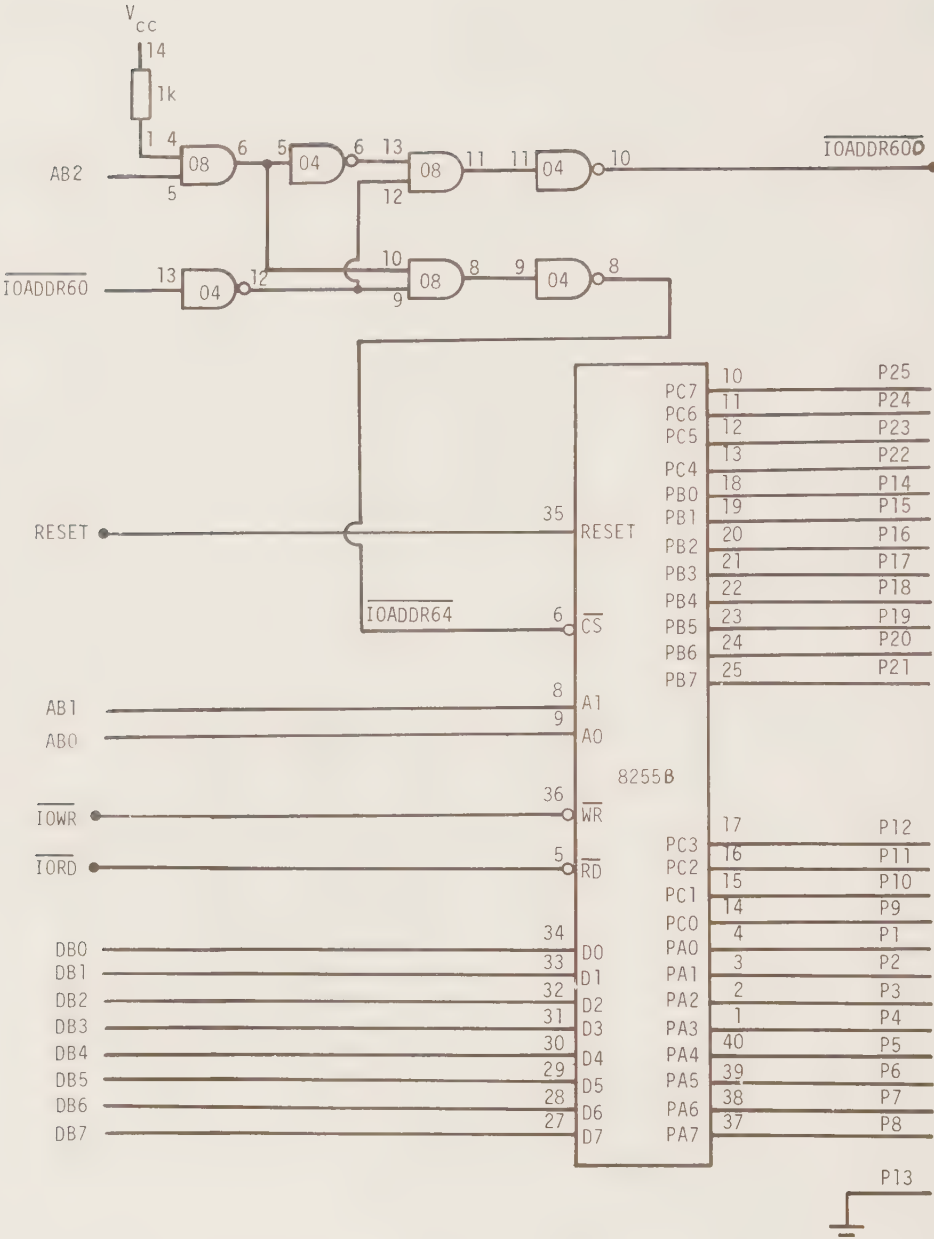


Fig 4-15 The magtape control and status board circuit diagram 2, the auxiliary I/O ports.

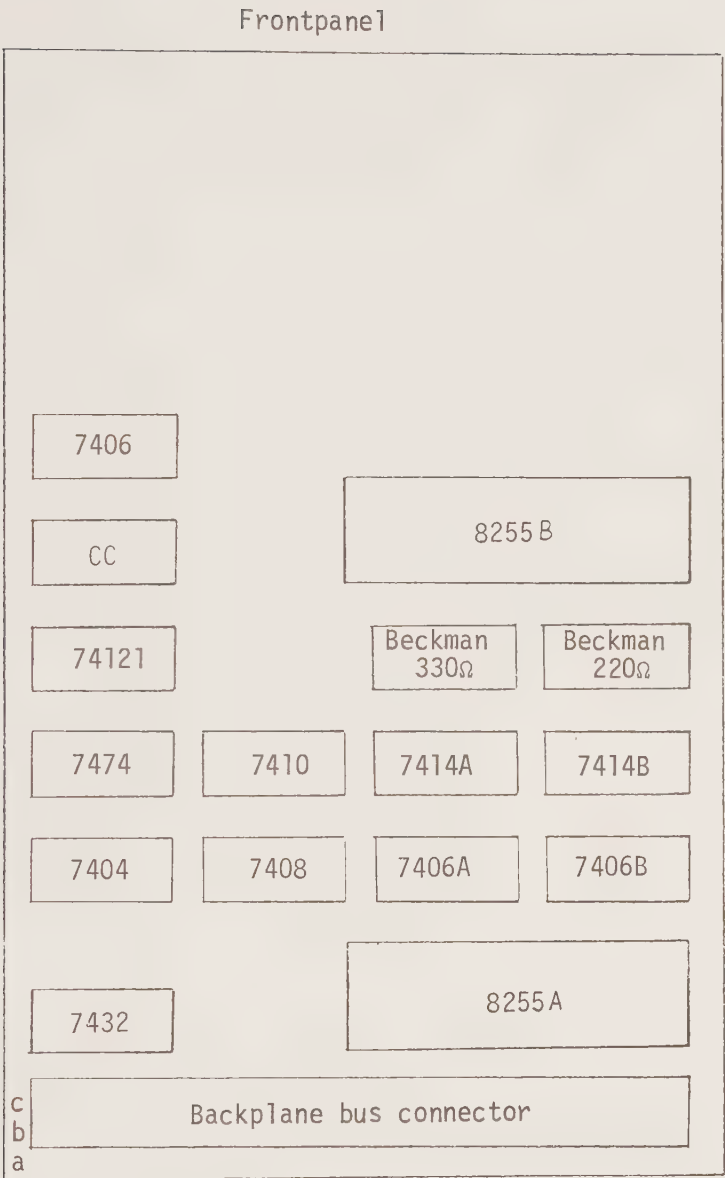


Fig 4-16 The magtape control and status board component layout. Board seen from component side.

Data direction as seen from the board	Pin number	Signal mnemonics	Short translation
=====			
Output	1	SLT0	SeLecT line 0
"	2	DDS	Data Density Select
"	3	OVW	OVerWrite
"	4	LOL	LOad On Line
"	5	SWS	SeT Write Status
"	6	RTH	ReaD ThresHold
"	7	OFFC	OFFline Command
"	8	SLT1	SeLecT line 1
"	9	SLT2	SeLecT line 2
"	10	SFC	SynChronous Forward Command
"	11	SRC	SynChronous Reverse Command
"	12	RWC	ReWInd Command
"	13	GND	GrouND
Input	14	RDY	ReaDY
"	15	HDI	High DensItY select (1600 bpi)
"	16	FPT	File ProTect
"	17	WEN	Write ENable
"	18	LDP	LoaD Point
"	19	RWD	ReWinDing
"	22	GAPDET	GAP DETect
"	23	RNG	RunniNG
"	24	EOT	End Of Tape
"	25	ONL	ON Line

Table 4-8 Pin assignment in female 25 pole Cannon connector on the front panel for magtape control and status marked P. Through this connector the control and status signals are sent to/received from the magtape station.

Data direction as seen from the board	Pin number	Signal mnemonics	Short translation
Input/Output	1	PA0	8255 port A bit 0
"	2	PA1	" " 1
"	3	PA2	" " 2
"	4	PA3	" " 3
"	5	PA4	" " 4
"	6	PA5	" " 5
"	7	PA6	" " 6
"	8	PA7	" " 7
"	9	PC0	" port C bit 0
"	10	PC1	" " 1
"	11	PC2	" " 2
"	12	PC3	" " 3
	13	GND	GrouND
Input/Output	14	PB0	8255 port B bit 0
"	15	PB1	" " 1
"	16	PB2	" " 2
"	17	PB3	" " 3
"	18	PB4	" " 4
"	19	PB5	" " 5
"	20	PB6	" " 6
"	21	PB7	" " 7
"	22	PC4	" port A bit 4
"	23	PC5	" " 5
"	24	PC6	" " 6
"	25	PC7	" " 7

Table 4-9 Pin assignment in female 25 pole Cannon connector on the front panel for auxiliary I/O ports, marked X. This connector was used during software development, but is presently not used in the scanner system.

4.2.8 Auxiliary functions

This chapter includes all the control circuitry that is not directly connected with any one of the major controllers or interfaces in the microprocessor system. Before a detailed description of each functional unit is given, a short summary of the different units and their function will be listed.

The address predecoder - divides the I/O address range into 16 subranges with 16 addresses in each.

The 16 one-bit pulse ports - output ports that issue a pulse instead of a static signal

The Control Data Bus (CDB) - an 8-bit PPI output port used as an additional bus for control signals

The HOME and END position detector circuitry

The drum motor control - start and stop of drum motor

The scanner light control - on and off control of the light source illuminating the drum in front of the optical scanner head

The stepper motor control

The real time clock (RTC)

The CMOS to TTL level converter

4.2.8.1 The address predecoder

The address predecoder shown in the upper half of Fig. 4-17, is located on the microprocessor board. A complete circuit drawing of this board is given in Appendix A4.2. The predecoder was added to the microprocessor system to reduce the size of the address decoder that must be present on each of the I/O boards. As the predecoder divides the 256 available I/O addresses into 16 subranges, each with 16 addresses, every I/O board only have to decode the 4 least significant bits of the address bus.

The 16 one bit pulse ports, located on the same board as the address predecoder are shown in the bottom half of Fig. 4-17. These output ports are named OUT00 - OUT0F, which is the same name as the instruction in the microprocessor which causes the output pulse. The pulses are used to issue reset-signals to the D flipflops on the interrupt request lines as described in chapter 4.2.3 and other similar signals when no information has to be added through the data bus.

The signal OUT00 makes it possible to reset the scanner system through software, without affecting the microprocessor. The other reset method is to activate the reset switch mounted on the microprocessor board front panel, but this will also reset the microprocessor.

4.2.8.2 The control data bus

The Control Data Bus (CDB) consists of 8 different control lines called CDB0-7. The CDB lines originate from a PPI (Programmable Peripheral Interface) located on the same board as the PIC (Programmable Interrupt Controller). A complete circuit diagram of the board including the CDB is given in Appendix A2.3.

The different control lines of the CDB have the following functions:

CDB0 scanner head movement determines stepper motor direction
"1" = reverse direction, "0" = forward direction

CDB1 Stepper motor start/stop control
"1" = stop stepping, "0" = start stepping

CDB2 Stepper motor step pulse generator select
"1" = Φ 2TTL signal, "0" = BSTB2 signal

CDB3 Duration of write strobe when writing on the tape
"1" = 1 μ s, "0" = 2 μ s

CDB4 Direction of magtape movement
"1" = reverse direction, "0" = forward direction

CDB5 Write amplifier reset strobe disable/enable. This signal controls whether the LRCC is added to the record on the tape during the write mode or not.
"1" = disable LRCC, "0" = enable LRCC

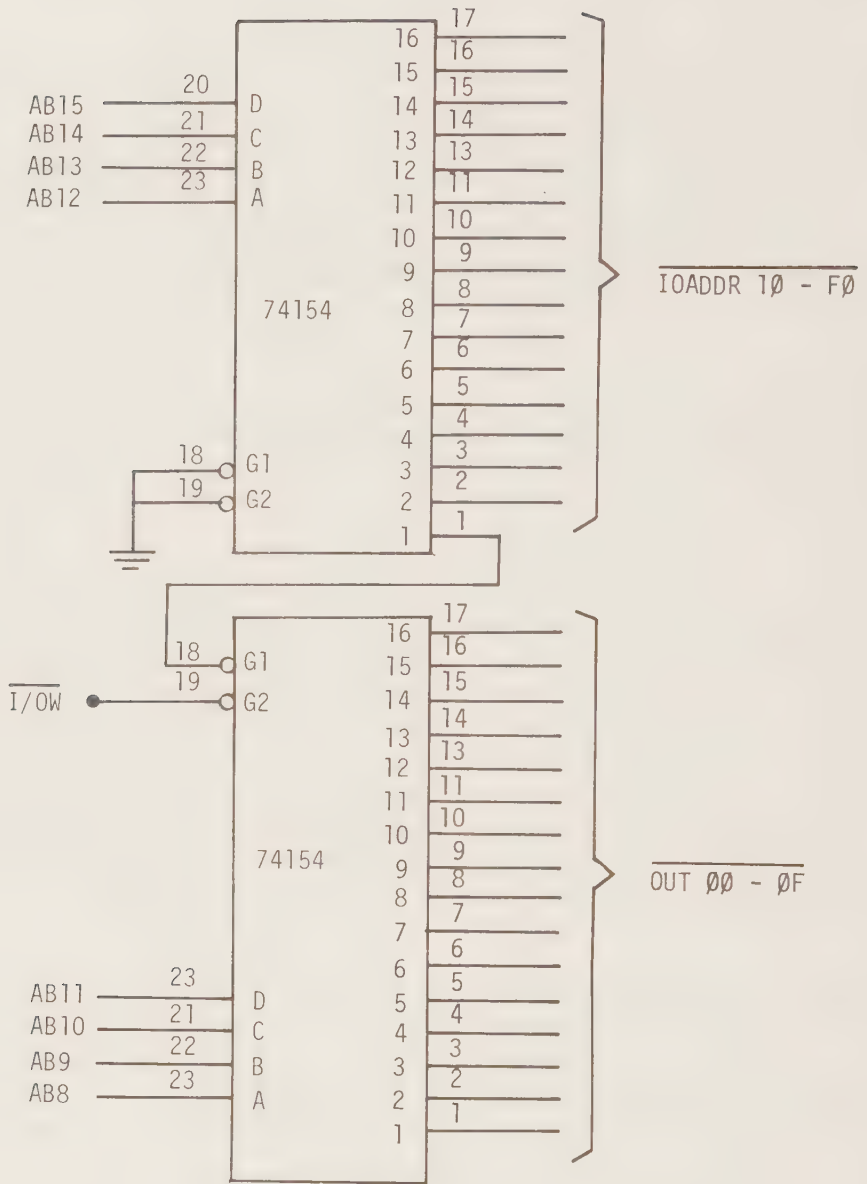


Fig 4-17 The address predecoder and sixteen 1 bit output pulse ports. The upper 74154, 4 to 16 decoder, divides the 256 available I/O addresses into 16 subranges, each with 16 consecutive addresses. The first subrange 00-0F (in hexadecimal notation) is used as sixteen 1 bit output pulse ports, as shown in the lower half of the figure, while the remaining 15 subranges are further decoded on the different boards.

CDB6 CRCC disable/enable. This signal controls whether the CRCC is added to the record on the tape during the write mode or not.
"1" = disable CRCC, "0" = enable CRCC

CDB7 Direction of the DMA transfers
"1" = DMA output enable, "0" = DMA input enable

4.2.8.3 HOME and END position detector

A block diagram of the HOME and END position detector circuitry is shown in Fig. 4-18. The detector is physically divided between two boards. The debounce circuitry is located on the image converter board 2 and the microprocessor interface is located on the magtape control and status board. The complete circuit diagram is hence divided into two parts, the debounce circuitry is depicted in Appendix A1.7, while the microprocessor interface is shown in chapter 4.2.7, Fig 4-14.

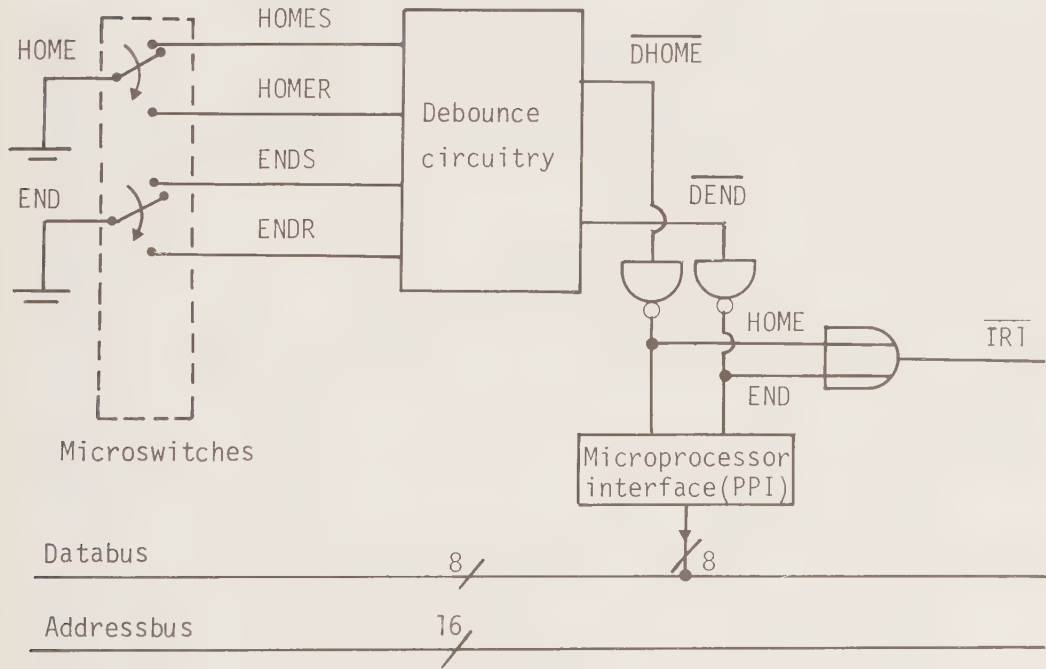


Fig 4-18 Block diagram of the HOME and END position detectors.

The HOME and END position microswitches, as most mechanical switches, generate rapid glitches when they switch from one position to another. These contact bounces might cause problems in the microprocessor system, and hence the debounce circuitry was added. The debounce circuitry reacts on the first negative going edge of the input signal and ignores the following bounces. The "clean" output signal from the debounce circuitry generates an interrupt request on the $\overline{\text{IRI}}$ interrupt request line. The interrupt service routine for level IRI reads the static signals HOME and END through the microprocessor interface to determine which of the two caused the interrupt request. A detailed description of the interrupt service routine is given in chapter 3.4.5.

4.2.8.4 Drum motor and scanner light control

The drum motor control and the scanner light control are shown as a block diagram in Fig 4-19. These control functions are located on the image converter board II, and a complete circuit diagram is given in Appendix A1.6.

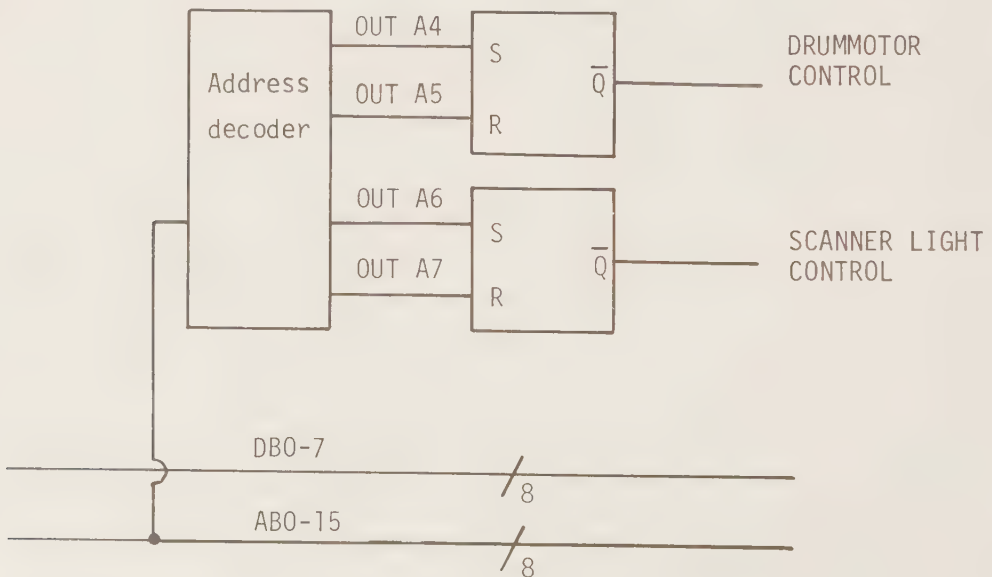


Fig 4-19 Block diagram of drum motor and scanner light control.

Four I/O addresses are used to perform the on/off switching of the drum motor and the scanner light. The I/O addresses are given below:

Start drum motor	OUT A4
Stop drum motor	OUT A5
Scanner light on	OUT A6
Scanner light off	OUT A7

The OUT-instruction asynchronously triggers the SR flipflops to one of two possible states.

4.2.8.5 Stepper motor control

A block diagram of the stepper motor control is given in Fig 4-20. The entire controller is located on the image converter board III, and a complete circuit diagram is given in Appendix A1.9.

The stepper motor is controlled by two signals, the DIR signal which selects the stepping direction according to the setting of CDB0, and the STEP signal which generates the step pulses for the stepper motor. During normal scanning operation, the programmable counter is set to divide the incoming signal with 165. It generates a square wave output. The BSTB2 signal from the shaft encoder circuit is selected as step pulse generator, and its 3360 pulses/revolution of the drum is divided by 165 resulting in 20 complete square waves when 3300 pulses are encountered. Before the 21st pulse is generated, the SLSTB signal from the shaft encoder clears the counter. At the beginning of the next scan line, the counter is started again from 0.

The start and stop of the stepper motor is only allowed prior to the beginning of a new scan line. This is necessary, as the interrupt service routines sometimes stops and restarts the stepper motor. If start and stop was allowed anywhere within the scan line, it would not be possible to restart the stepper motor without error in the scanned image. Therefore the start/stop signal, CDB1, is gated through the D flipflop. Any start or stop command during a drum revolution will not be acknowledged by the programmable counter until the SLSTB signal clocks the D flipflop.

In some cases (c.f. chapter 3.5.1) it is necessary to move the scanner head while the drum is not rotating. This could be a problem, as both the BSTB2 and the SLSTB signals are inactive. Therefore the system clock, Φ_{TTL} , is added as an alternate step pulse generator. The OUT08, OUT09 and OUT0D signals are added to control the stop and start of the stepper motor independent of the SLSTB signal. These signals are generated by the OUT 08, OUT 09 and OUT 0D instructions in the microprocessor through the address predecoder described in chapter 4.2.8.1

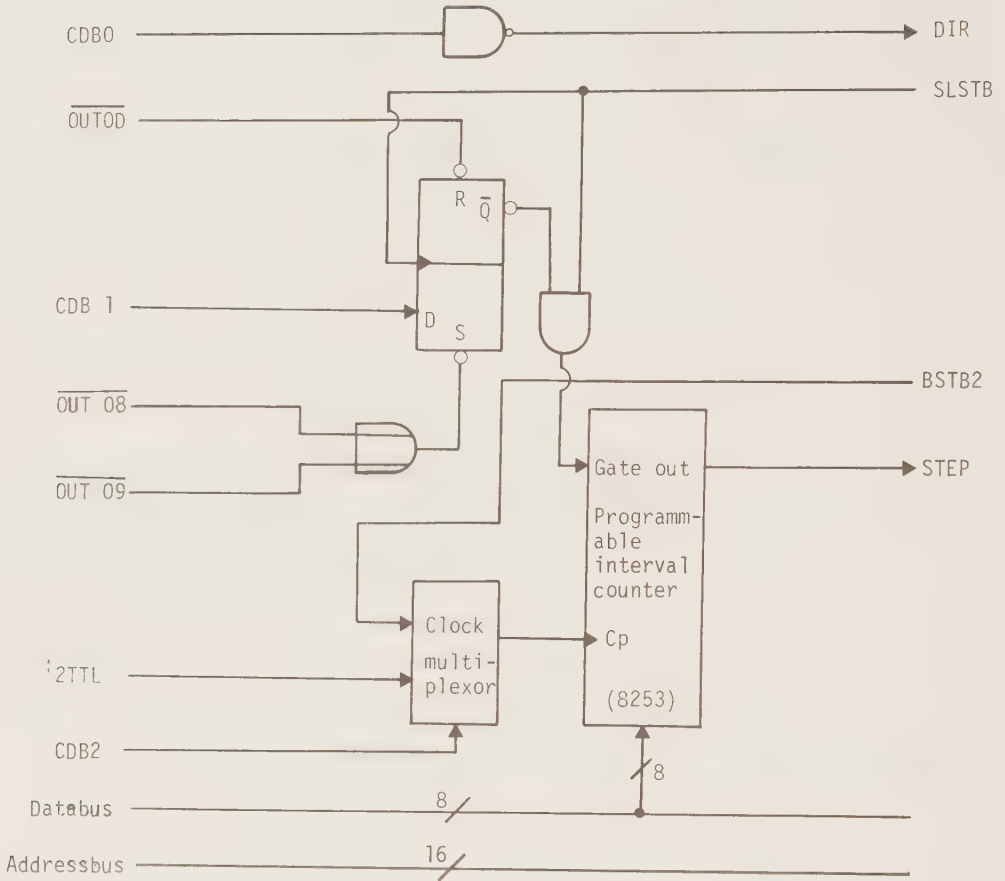


Fig 4-20 Block diagram of the stepper motor control.

4.2.8.6 Real time clock

The Real Time Clock, RTC, is located on the same board as the PIC (Programmable Interrupt Controller). A complete circuit diagram is given in Appendix A2.2 The RTC is based on the 8253 PIT (Programmable Interval Timer), and operates as an autonom square wave generator with a cycle time of 10 ms. The positive going edge of the square wave generates an interrupt request on the IR0 interrupt request line. The interrupt service routine checks if the last input from the operator terminal is a control-A. (The control-A character is generated by simultaneously depressing both the control and the A key on the keyboard.) If it encounters a control-A, all non-interruptdriven routines are terminated. This makes it possible to stop the execution of a routine without affecting the normal scanner operation. In the scanner system only three routines described in chapter 3.3 and 3.5 are affected by the RTC, namely the scanner initiation routine, the scanner head positioning routine and the Dither threshold preload routine.

The execution time of this interrupt service routine is less than 60 μ s in every 10 ms interval. Hence this routine only uses $(60/10000)*100=0.6$ % of the available processing time.

4.2.8.7 CMOS to TTL converter

The CMOS to TTL converter shown in Fig 4-21 is located on the micro-processor board. A complete circuit diagram of this board is given in Appendix A4.2.

The CMOS to TTL level converter was required to operate the transparent DMA controller. The 8224 Clock circuit, which is a part of the microprocessor, generates the Φ_1 and Φ_2 clocks at CMOS levels, but only the Φ_{2TTL} clock at TTL levels. As both clocks are needed at TTL levels, this converter was added.

In spite of the larger input voltage of Φ_1 , the collector of the transistor is held within the -0.2 to +5.2 V voltage range set by the two germanium diodes and their forward voltage drop of 0.2 V. The 74367 schmitt trigger is used to transform the collector voltage of the transistor to standard TTL levels.

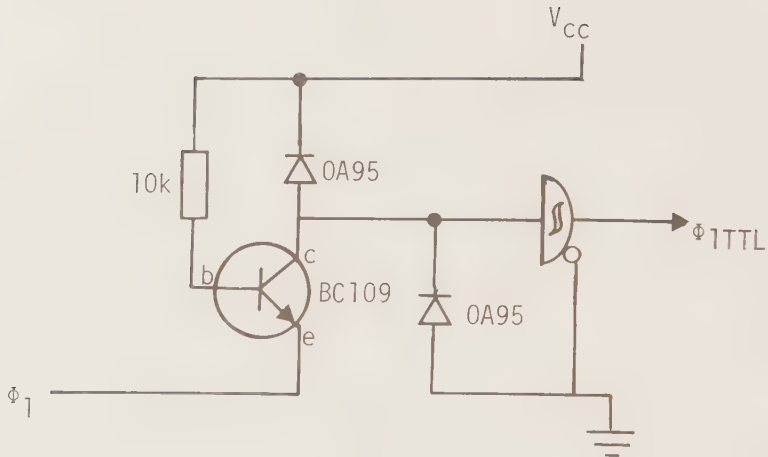


Fig 4-21 The CMOS to TTL level converter circuit diagram. The collector of the transistor is restricted by the germanium diodes to a voltage range between $V_{CC}+0.2$ V and $GND-0.2$ V, independent of a higher input voltage range. (0.2 V is the Ge diode forward voltage drop.)

4.2.9 The Operator Terminal Interface

The operator communication is based on the polling method mentioned in chapter 2.3. The program executing in the microprocessor sends a message to the operator terminal, and thereafter polls the terminal input waiting for the operator to respond to the message. An exception of this polling method is the interrupt controlled routine that handles the control A character, c.f. chapter 4.2.8.6.

The operator terminal interface board shown in Fig. 4-22 also contains another interface for serial communication with a host computer. This latter interface, shown in Fig. 4-23, was mainly used during software development. The component layout of this board is given in Fig. 4-24.

The interfaces are based on the 8251 USART (Universal Synchronous/Asynchronous Receiver/Transmitter). This communication controller sends and receives data as serial bit streams and handles the packing and unpacking of the bytes.

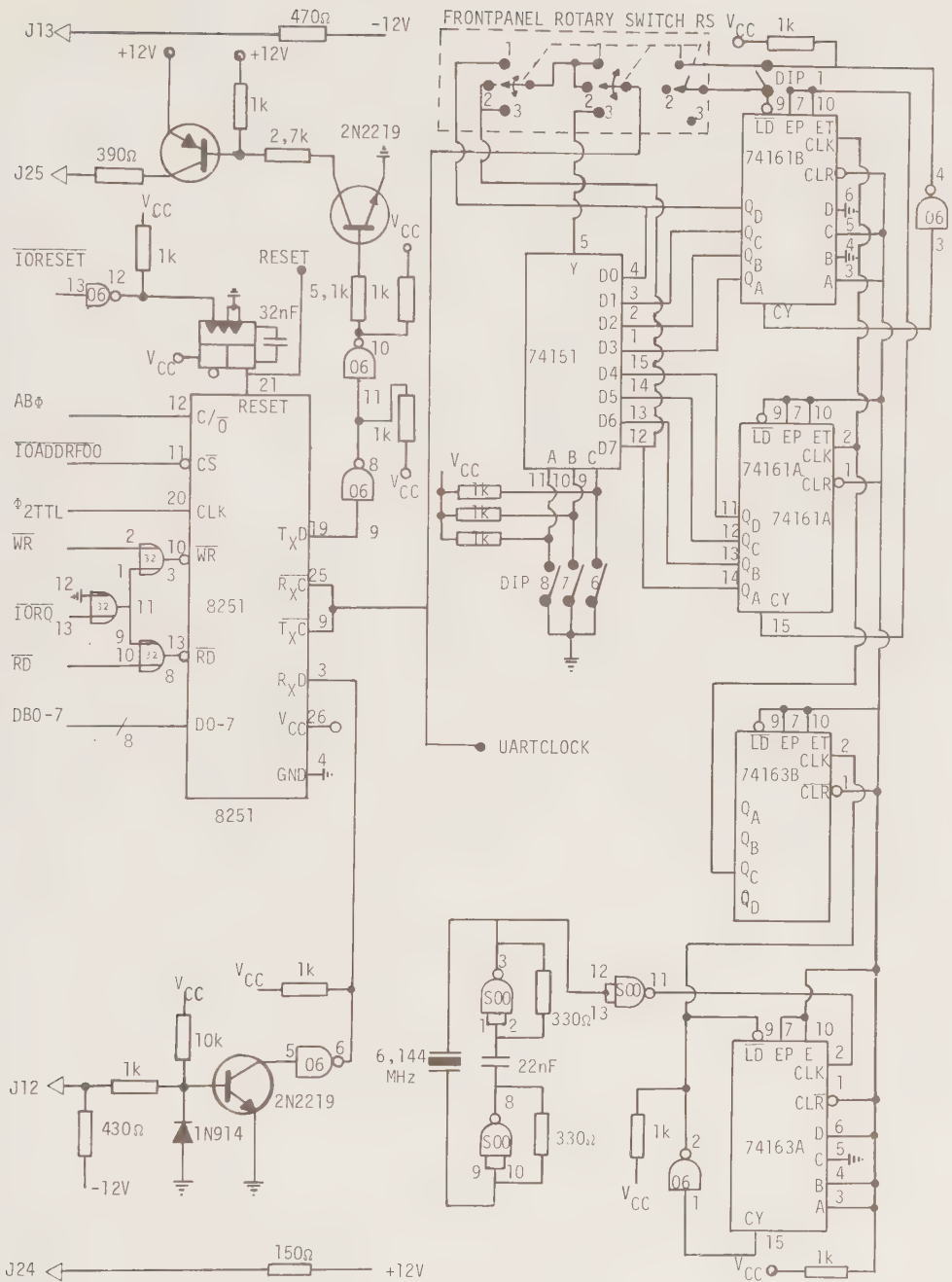


Fig 4-22 The operator terminal interface board circuit diagram 1, the baud rate clock and the operator communication.

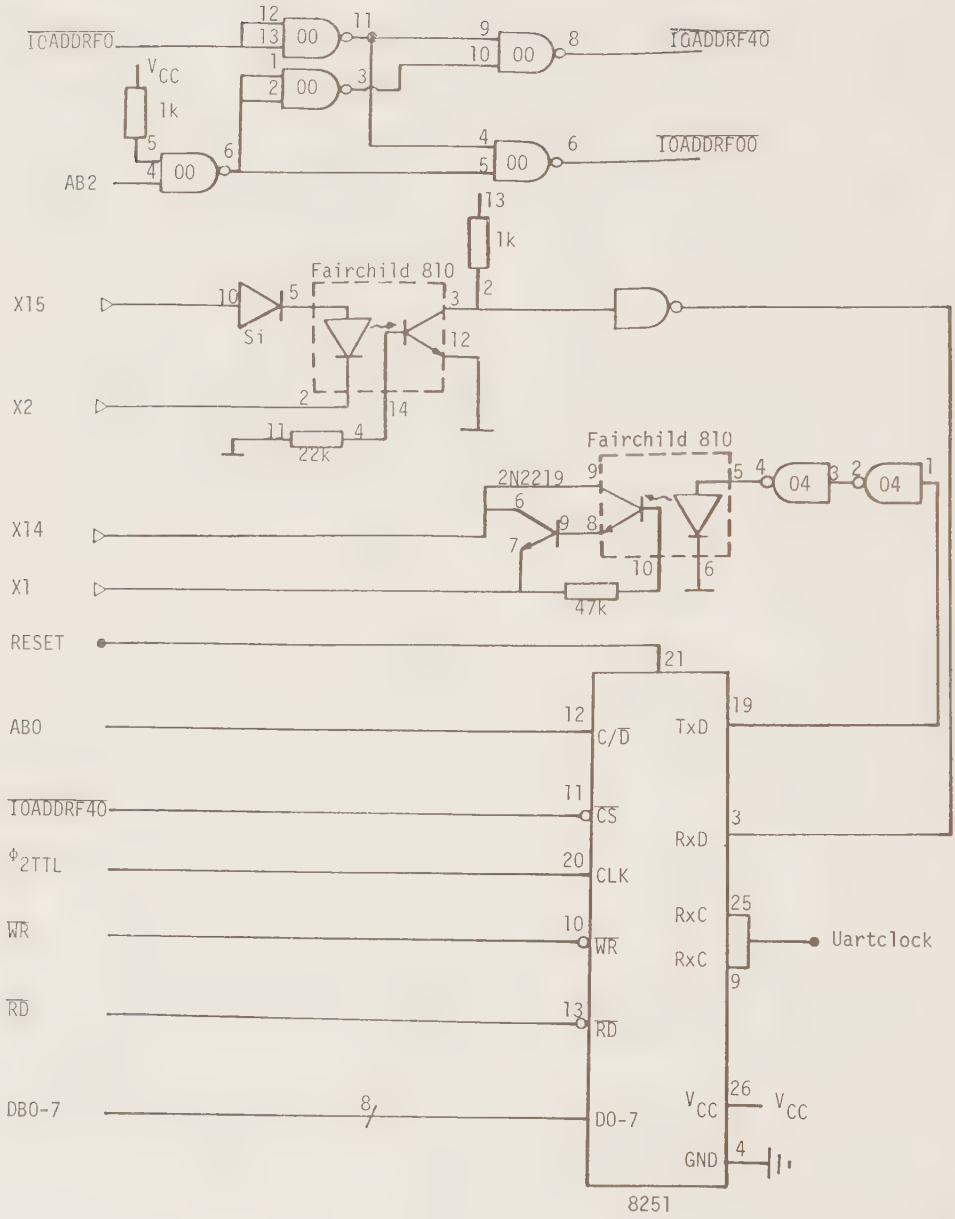


Fig 4-23 The operator terminal interface board circuit diagram 2, the host computer communication.

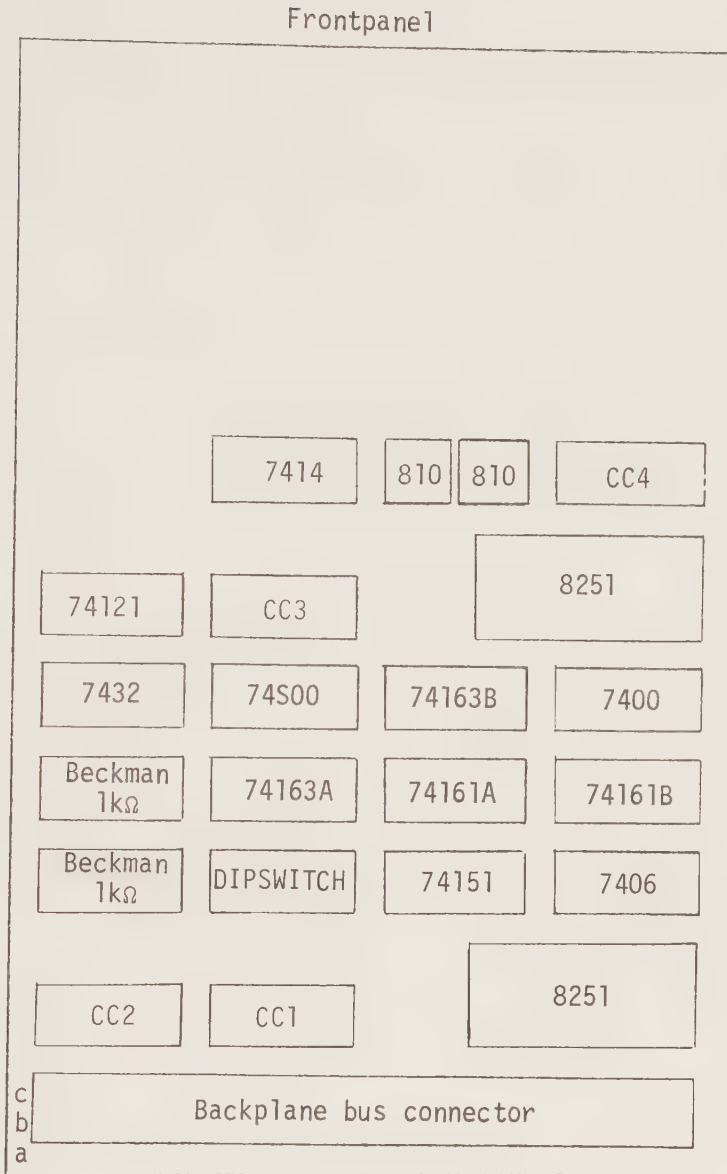


Fig 4-24 The operator terminal interface board component layout. Board seen from component side.

The USART operation in transmit mode can be described as follows:

The byte to be transmitted enters the USART as 8 parallel bits, the USART adds a start bit at the beginning and thereafter sends the 8 bits one by one in a serial bit stream. After the last bit in the byte is transmitted an extra parity bit can be sent and one or two stop bits must be sent.

The USART receiving this information acts as follows:

The start bit alerts the USART that data is coming, and the USART reads the following 8 bits and perhaps also the parity bit if this is specified. Thereafter it makes the byte available on its parallel outputs, and sets a bit in its status register to indicate that data is ready to be retrieved. The stop bits are merely used as spaces between bytes.

In the scanner system the USARTs are operated in asynchronous mode, which means that each USART has its own clock frequency. This requires accurate clock frequency generators and therefore the transmit and receive clocks in the microprocessor system are crystal controlled.

The output frequency from the crystal oscillator is 6.144 MHz. As this is much too high a frequency for the USARTs, a dividing network is added. The dividing network consists of four counters 74163 and a multiplexor 74151 as shown in Fig. 4-22.

This network makes it possible to use different baud rates for communication. Three transmission speeds can be directly selected using the rotary switch <RS> mounted on the board front panel.

The possible setting of the RS are:

- position 1 : 110 baud
- position 2 : 9600 baud
- position 3 : baud rate preset on the board through dip switches

The presettable baud rate is controlled by the DIP switches S1, S6, S7 and S8, as shown in Table 4-10. All baud rates given in Table 4-10 requires that the USART is programmed to divide the incoming clock frequency by 16.

The operator and host computer communication use the 20 mA current loop technique. This technique has a very high noise immunity compared to other serial communication methods using voltage.

Dip switches:				Preset
S8	S7	S6	S1	baud rate
=====				
closed	closed	closed	open	75
"	"	"	closed	110
"	"	open	open	150
"	open	closed	"	300
"	"	open	"	600
open	closed	closed	"	1200
"	"	open	"	2400
"	open	closed	"	4800
"	"	open	"	9600

Table 4-10 Baud rate selection for the rotary switch, RS, position 3.

In a current loop communication only one of the units can supply the current for the communication. This unit is called the active unit, and the other is called the passive unit. Normally the computer/processor is the active unit while the terminal or equivalent is the passive unit. Therefore the USART used for operator terminal communication is working as the active unit, while the USART used for host computer communication is working as a passive unit. As an extra precaution the electric lines going between the host computer and the scanner system are optoisolated. Hence electrical hazards, probable during the hardware development, will not reach the host computer.

Both serial interfaces are accessible in one 25 pole female CANNON connector mounted in the board front panel together with the rotary switch RS. The pin assignment is given in Table 4-11.

Pin number	Function	
=====		
1	transmit	- to host computer (passive)
2	receive	- from host computer (passive)
12	receive	- from operator terminal (active)
13	transmit	- to operator terminal (active)
14	transmit	+ to host computer (passive)
15	receive	+ from host computer (passive)
24	receive	+ from operator terminal (active)
25	transmit	+ to operator terminal (active)

Table 4-11 Pin assignment in 25 pole female CANNON connector for two 20 mA current loop serial interfaces.

4.2.10 The Microprocessor

The microprocessor is the part of the scanner system which participates in most of the activities. It has a master function during initiation, and more of a slave function throughout the scanning operation, as all tasks performed by the microprocessor are initiated by the PIC.

The block diagram shown in Fig 4-25 depicts the fundamental parts of the microprocessor. A complete circuit diagram of this board is given in Appendix A4.2. The actual data processing takes place in the 8080A microprocessor chip, while the 8224 clock circuit generates the two processor clocks and controls the timing of the system. The 8228 system controller generates the system control signals, such as read and write signals for memory and I/O. The function of the fundamental parts of the microprocessor will not be commented on as it is beyond the scope of this report to describe the microprocessor internal operation.

To increase the loading capabilities of the address and data busses, and to allow for the transparent DMA controller to use the busses, additional tristate buffers were added. These tristate buffers are controlled by the DMA controller signal AEN.

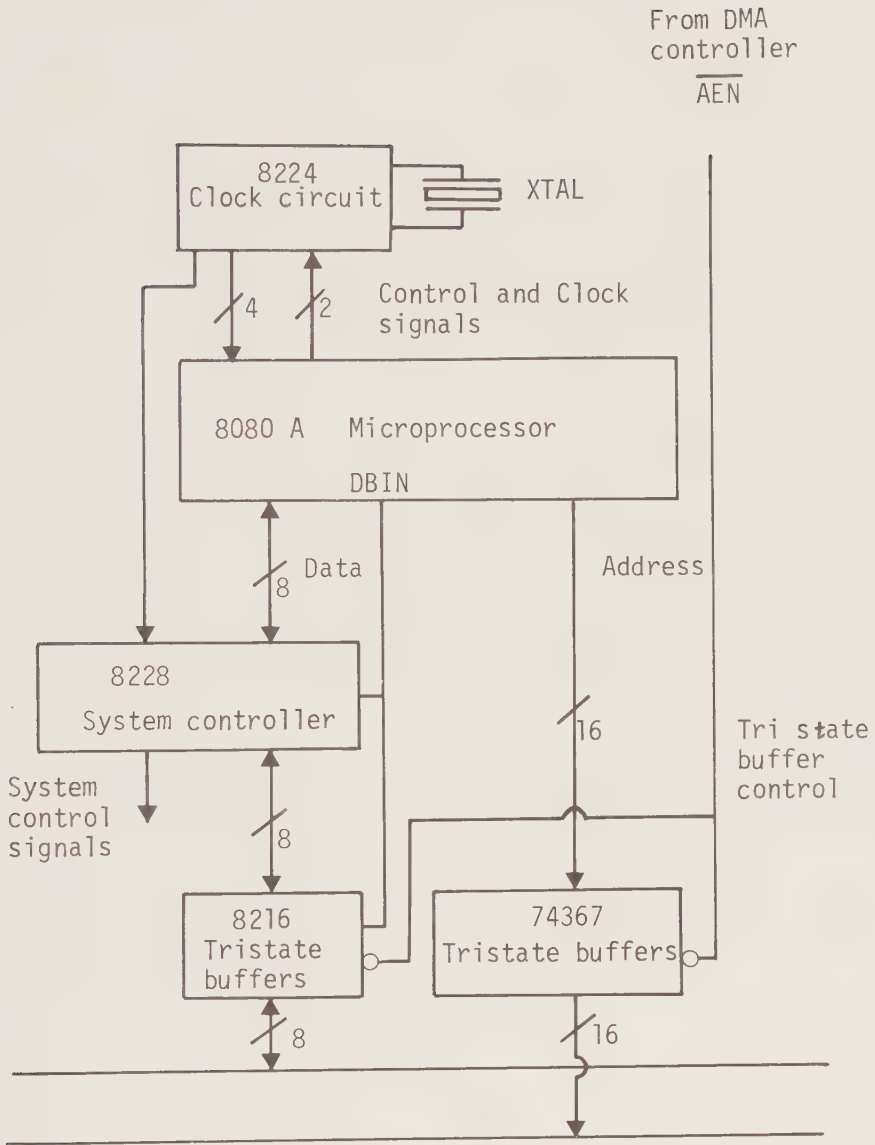


Fig 4-25 Block diagram of the microprocessor.

4.2.11 The microprocessor ROM

The Read Only Memories used in the microprocessor system are 2708, 1 kbyte EPROM chips. They are almost pin compatible with the 4118 static memory chips used in the microprocessor system RWM, and hence the same board can be used with minor modifications. The circuit diagram is shown in Fig. 4-26 and is essentially a duplicate of Fig. 4-9. When using ROM chips the board has to be altered as follows:

The 74138, 3 to 8 decoder, is inserted in the socket marked A, as shown in Fig 4-26.

The 74138 decoder resolves the address from the bus in increments of 1 kbyte, within the 8 kbyte memory area resolved by the 7485 4-bit comparator.

The 16 pin component carrier (CC) with the pins 4, 7, 9, 10, 11, 12, 13, 14 and 15 interconnected by wires is inserted in the socket marked B and thereby holds the programming pin on all EPROMs at "0" as no programming of the EPROMs is possible on these boards.

The dip switches S5 and S6 are open and the dip switches S7 and S8 are closed. S7 and S8 supplies the 2708 EPROM chips with the two additional voltages they need to operate, namely the VDD (+12 V) and VBB (-5 V).

The board is now ready to accept ROM chips. Before the board is inserted in the microprocessor system some additional setting must be carried out. These settings are identical for the ROM and RWM chips. Therefore this procedure will not be discussed any more, as it is already described in chapter 4.2.4.

The scanner system software is located in approx. 2 kbytes of ROM. This includes some of the utility routines, used only by the scanner system. But as the microprocessor also has a small operating system, an editor/assembler, an inverse assembler and a basic interpreter two memory boards containing 16 kbyte of ROM are used in the system.

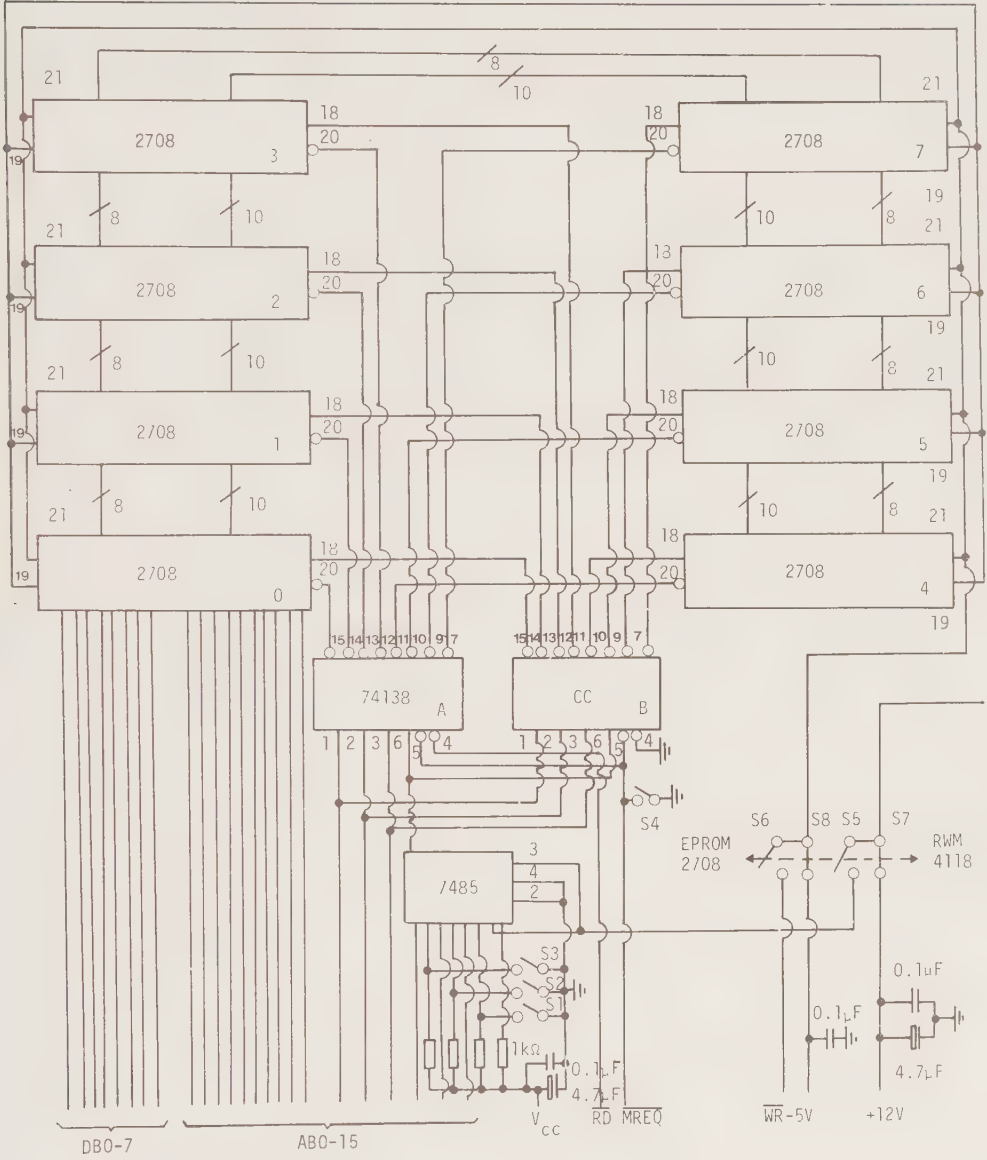


Fig 4-26 The microprocessor system ROM circuit diagram.

4.2.12 The 2708 EPROM programmer

The EPROM programmer board shown in Fig 4-27 with component layout as in Fig 4-28 was originally used as a programmer during software development. In the present system, however, this board is used every time a new Dither threshold matrix is preloaded into the microprocessor system RWM (c.f. chapter 3.5.2). The 2708 EPROM containing the Dither threshold matrices is inserted in the front panel socket of this board.

Besides the PPI (Programmable Peripheral Interface) handling the address and data to/from the front panel socket, this board contains the logic for generating the write pulses used when programming the EPROMs. It also has its own software stored in a 2708 EPROM located on the board. The start address is E000 in hexadecimal notation. The functions of the subset of this software used in the scanner system are described in chapter 3.5.2. As both hardware and software is located on this board, it can be used in other microprocessor systems with the same bus structure.

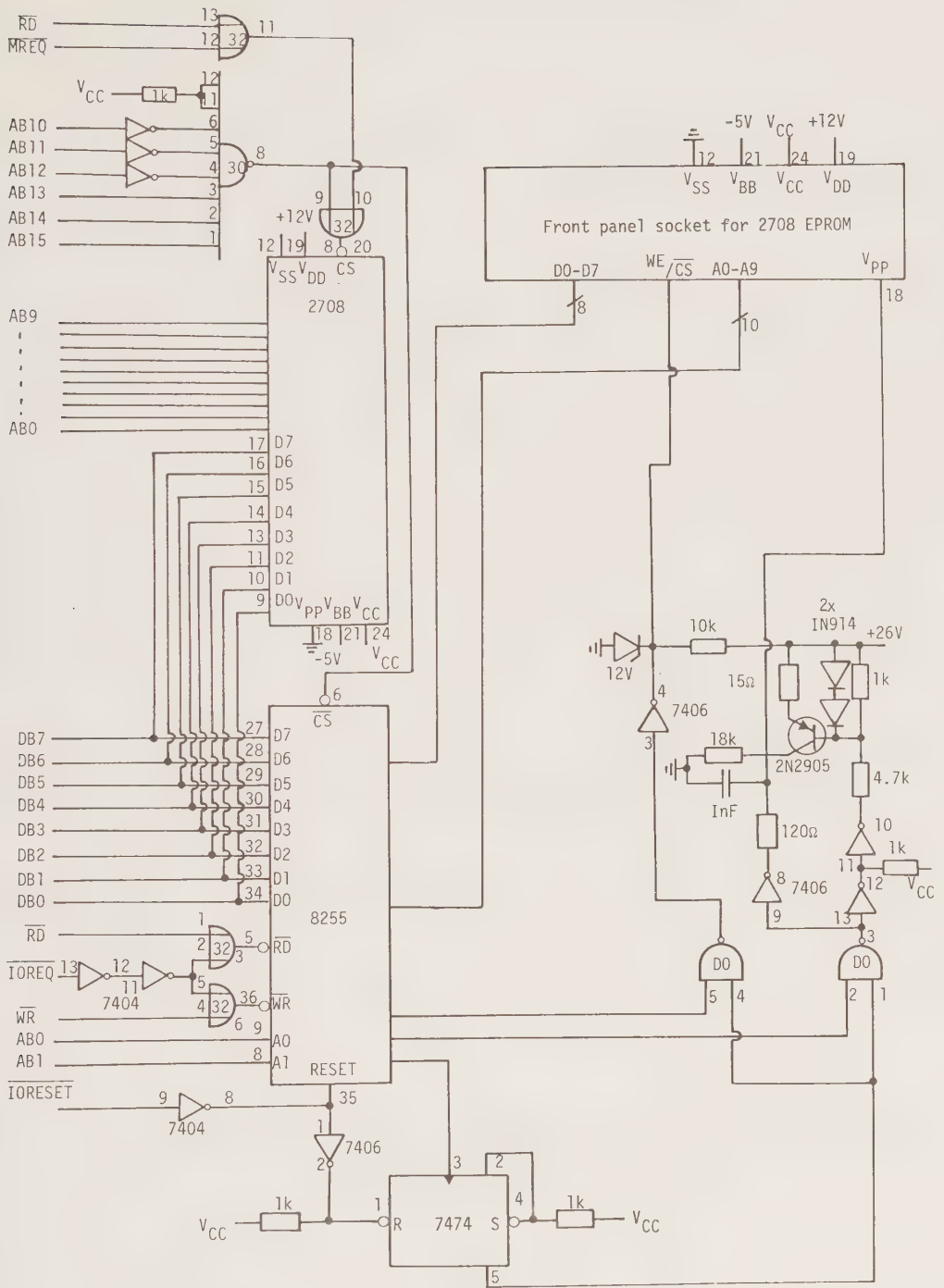


Fig 4-27 The 2708 EPROM programmer circuit diagram.

Frontpanel

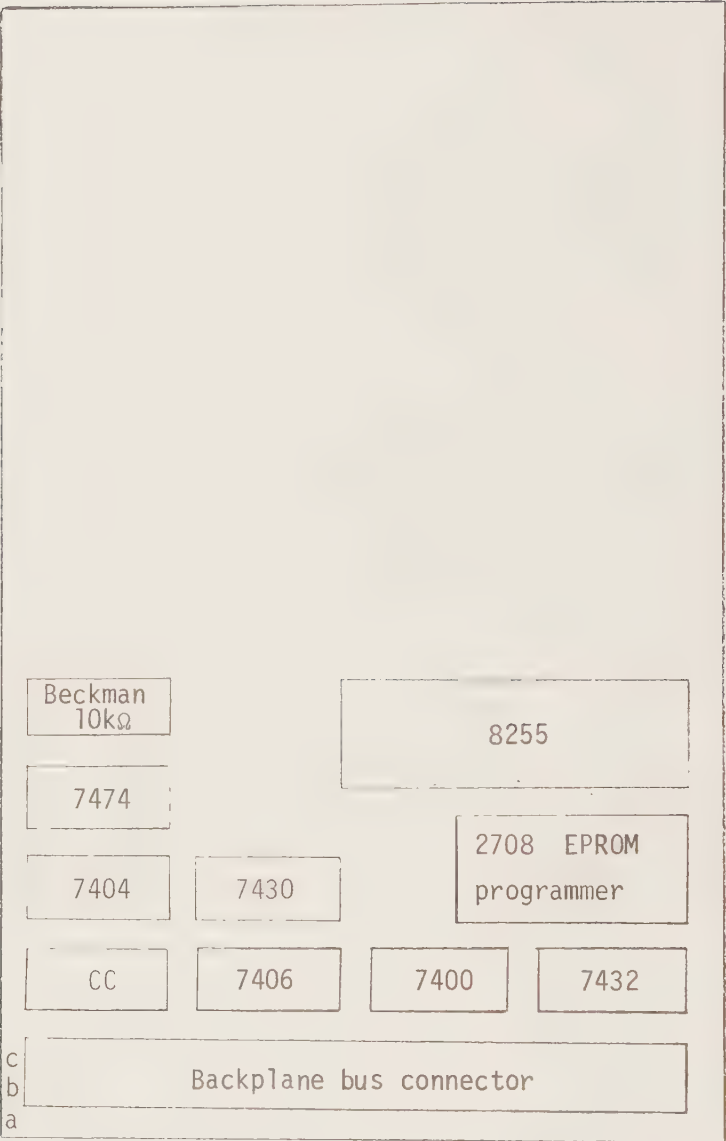


Fig 4-28 The 2708 EPROM programmer board component layout. The EPROM to be handled by the programmer is inserted in a socket on the board front panel. Board seen from component side.

ACKNOWLEDGEMENTS

I wish to express my sincere gratitude to Professor Hellmuth Hertz, Head of the Department of Electrical Measurements, Lunds Institute of Technology, for initiating this work as well as for his stimulating guidance throughout the work.

The keen interest in my work shown by all colleagues has created an inspiring atmosphere at the Department. I especially wish to thank my colleague Dr. Jan Ove Nilsson, who participated in the early development phase of the electronic control system described in this paper, for his continuing interest and advice. Thanks are also due to my friend Mr. Olle Hydbom who developed a small operating system and several utility routines in the microprocessor system which greatly simplified the development of the scanner system software. Mr. Olle Hydbom together with Mr. Hans Resmark, also constructed parts of the microprocessor hardware as their diploma thesis.

The skillful assistance by Mr. Lennart Nilsson, Mr. Jörgen Carlsson and Mr. Tomas Persson in the workshop has been invaluable throughout the work.

I also want to thank Mrs. Anita Borné, Mrs. Lena Carlsson and Mrs. Elly Schlyter for their skill, care and attention when preparing the drawings. Finally, I wish to thank Mrs. Margaret Jansson for her enthusiastic concern and help throughout this paper.

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APPENDIX A

In this report the description of the scanner system hardware is divided into functional units, such as controllers and interfaces. Unfortunately the physical division of the scanner system into it's circuit boards is different. Some controllers are located on several circuit boards, while others share a circuit board. The reason for these combinations of controllers on single boards are purely technical to reduce the number of boards and interconnections.

Hence, instead of adding the complete circuit drawing of each circuit board when it is referred to in this report, all circuit diagrams with several different functions are added in Appendix A1 through A4 as shown below.

The image converter board I	
The image converter board II	
The image converter board III	A.1. 1-12
The programmable interrupt controller	
The DMA controller registers and counters	A.2. 1-3
The magtape formatter board	A.3. 1-5
The microprocessor board	A.4. 1-2

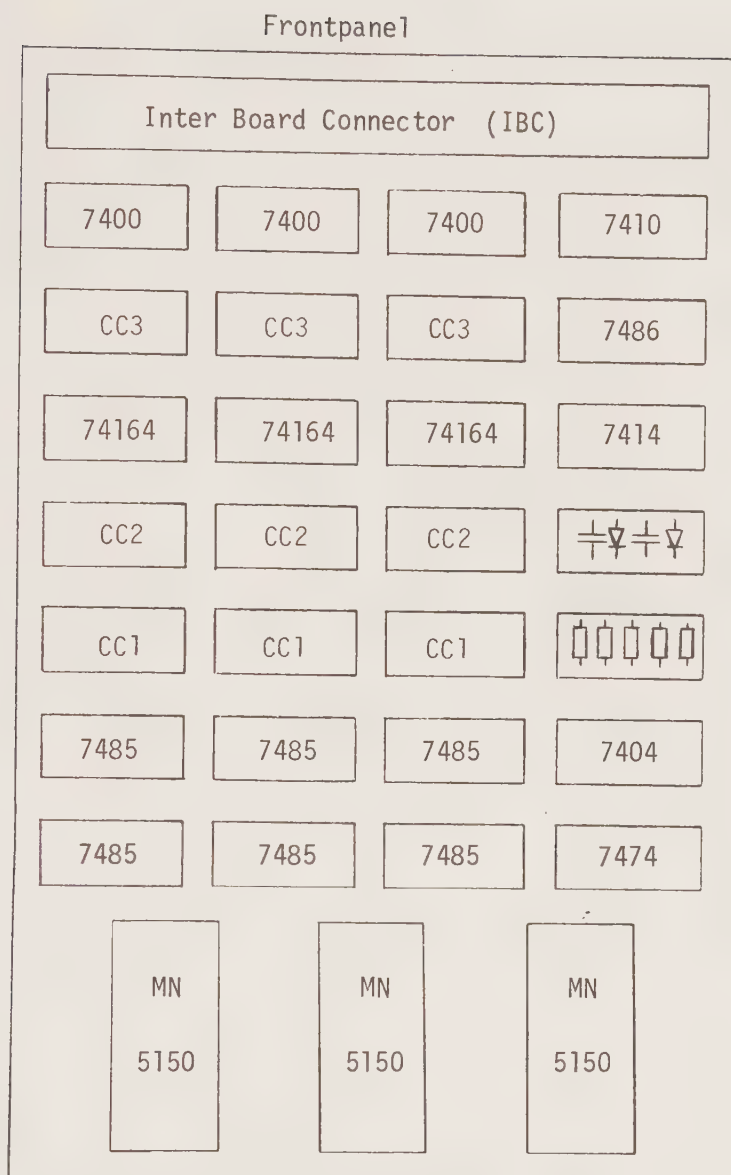


Fig A1-1 The image converter board I component layout. Board seen from component side. This board is not connected to the microprocessor system backplane bus. Instead all communication is directly to the image converter board II, through the Inter Board Connector (IBC).

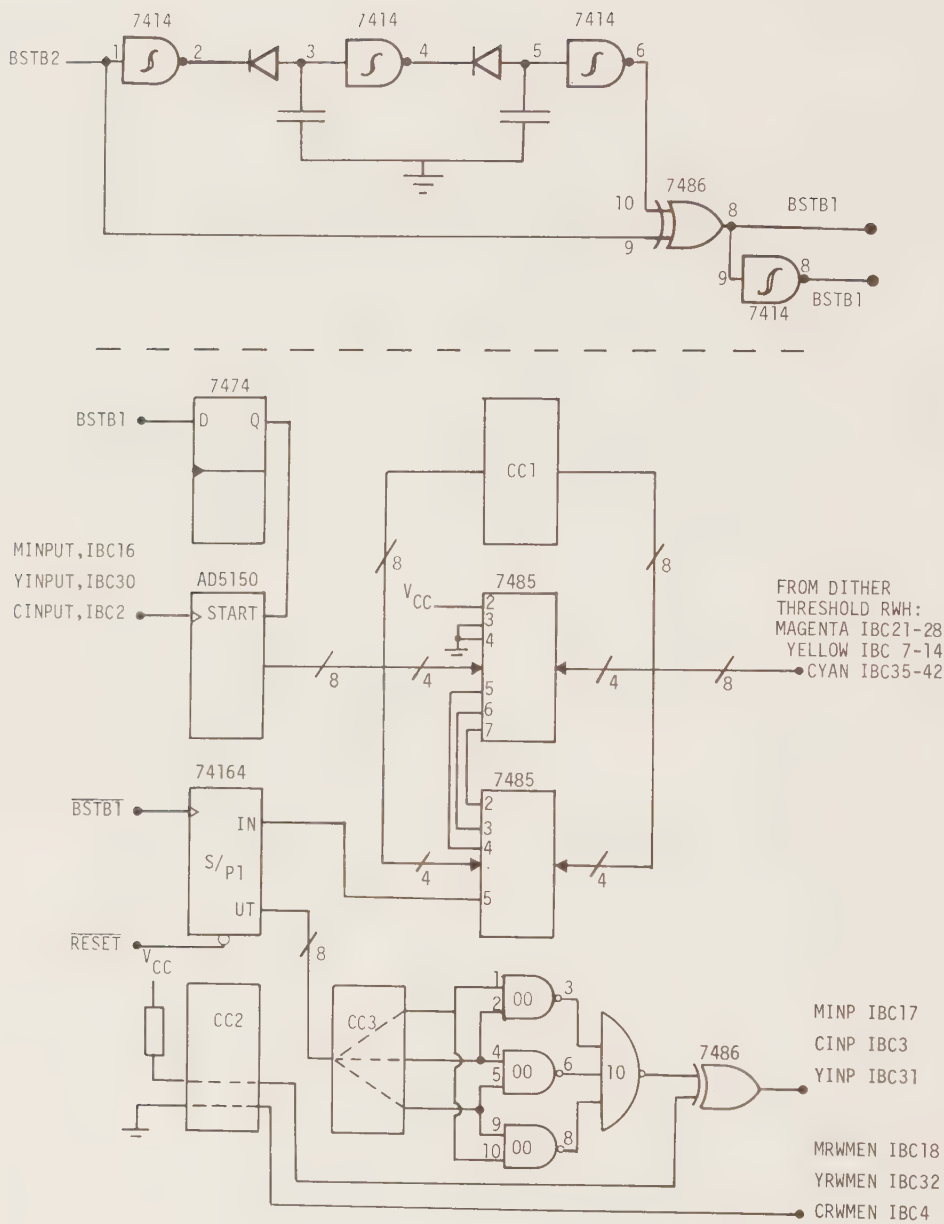


Fig A1-2 The image converter board I circuit diagram. This board includes the A/D converters and the comparator circuitry. The electronic circuitry below the dotted line exists in triplicates, one for each of the three color channels.



Fig A1-3 The image converter board II component layout. Board seen from component side. This board communicates with both the microprocessor backplane bus and the inter board connector (IBC).

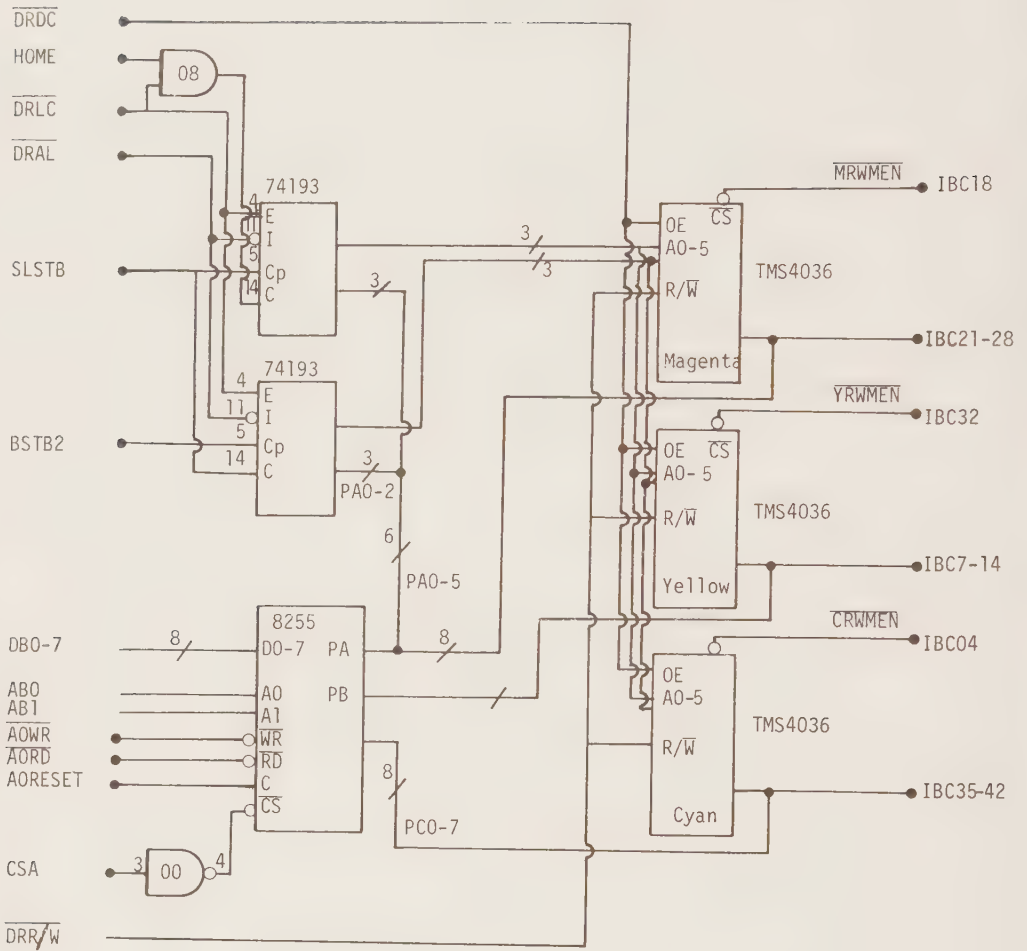


Fig A1-4 The image converter board II circuit diagram 1. This diagram includes the Dither threshold RWMs with address and data bus connections to the microprocessor system. All connections to/from the image converter board I are marked IBC.

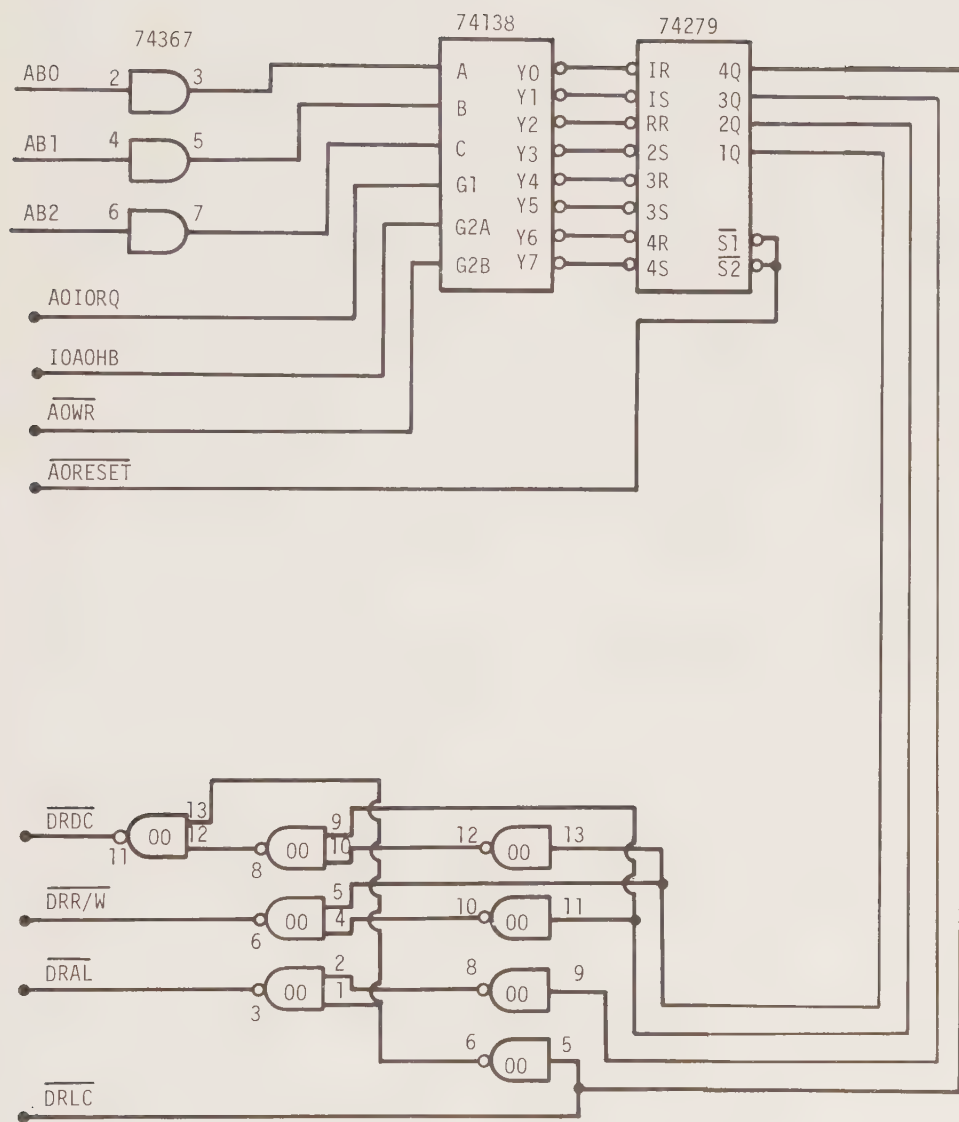


Fig A1-5 The image converter board II circuit diagram 2. This diagram includes the Dither threshold RWM control logic used when loading and reading the threshold information to/from the Dither threshold RWMs.

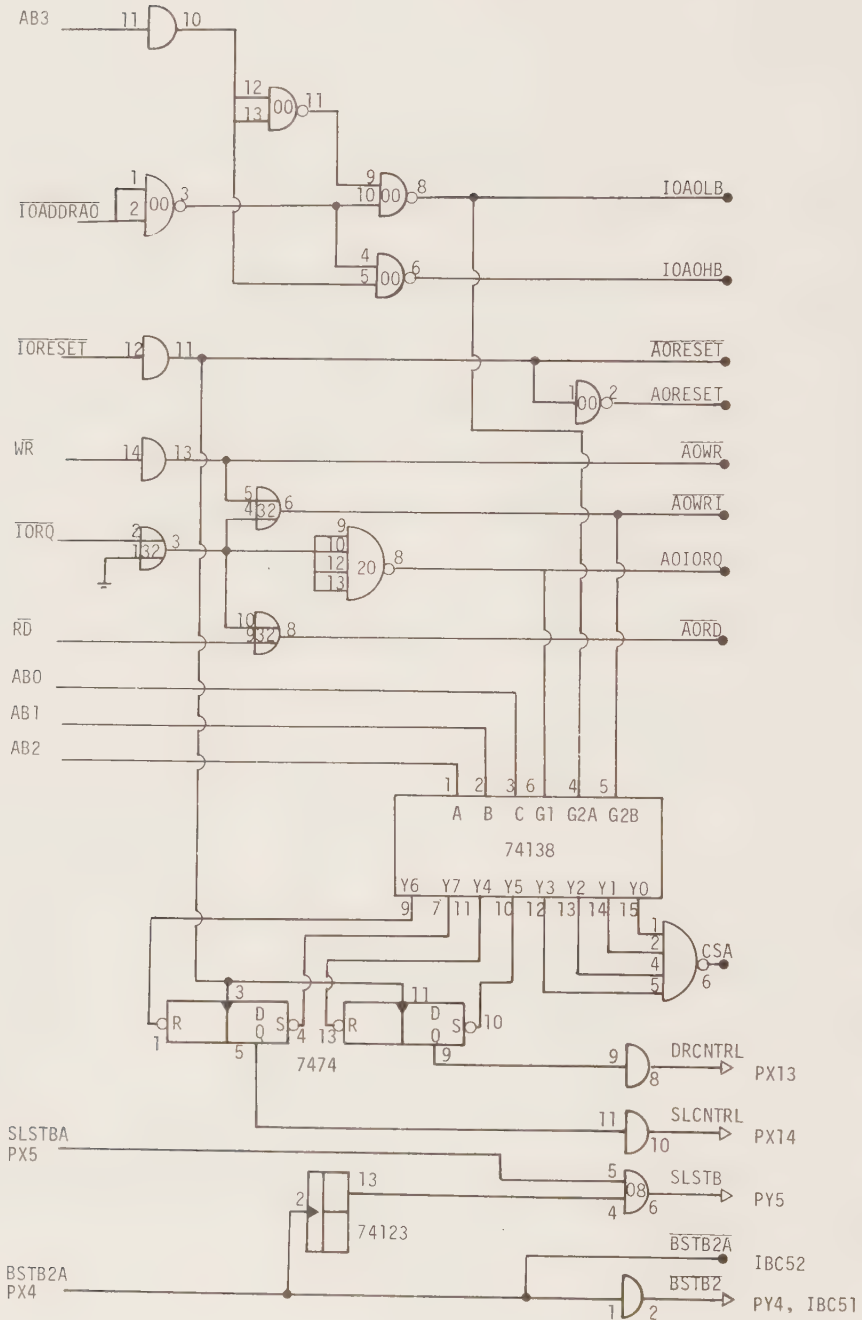


Fig A1-6 The image converter board II circuit diagram 3. This diagram includes the address decoder for the board, the drum motor and scanner light control circuitry.

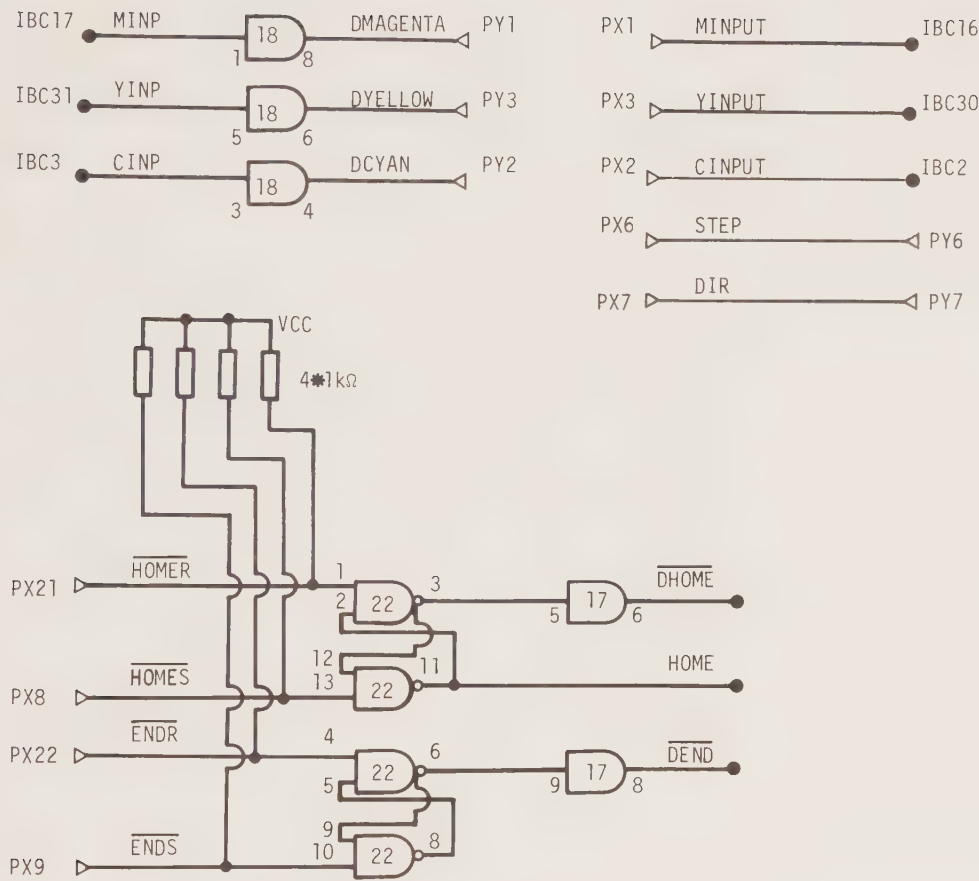


Fig A1-7 The image converter board II circuit diagram 4. This diagram includes the HOME and END position debounce circuitry and a set of interconnections between the IBC and the front panel connectors.

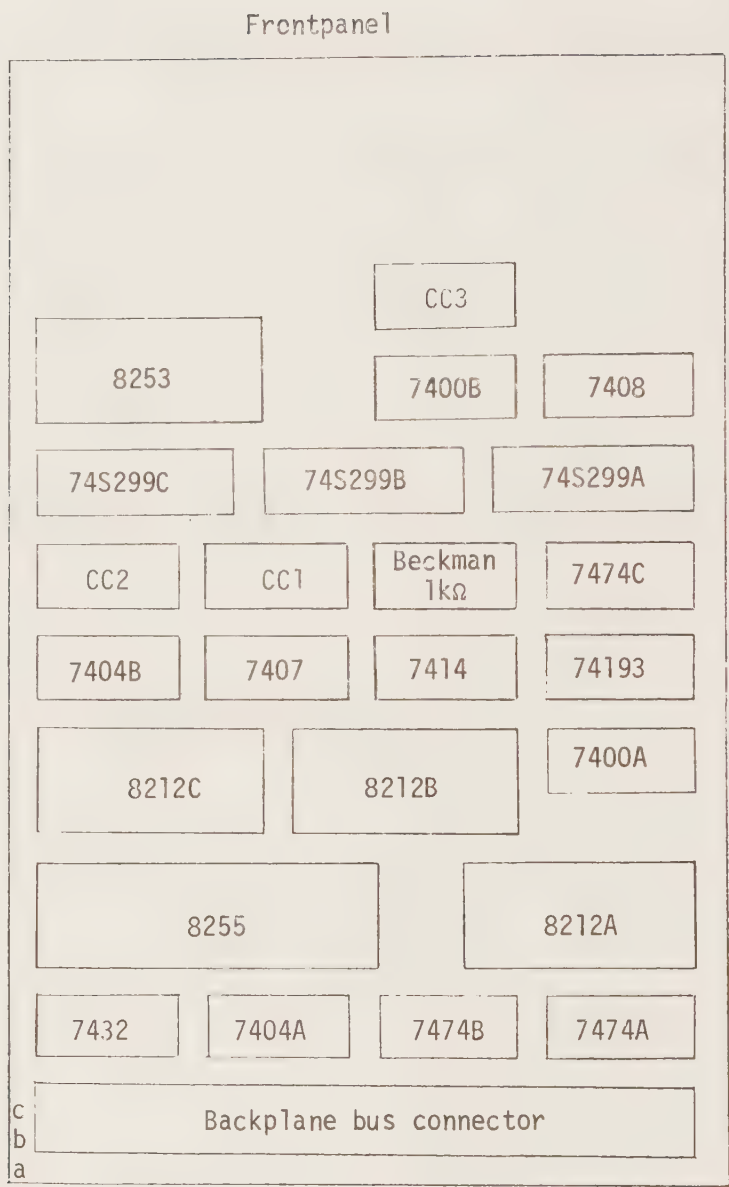


Fig A1-8 The image converter board III component layout.
Board seen from component side.

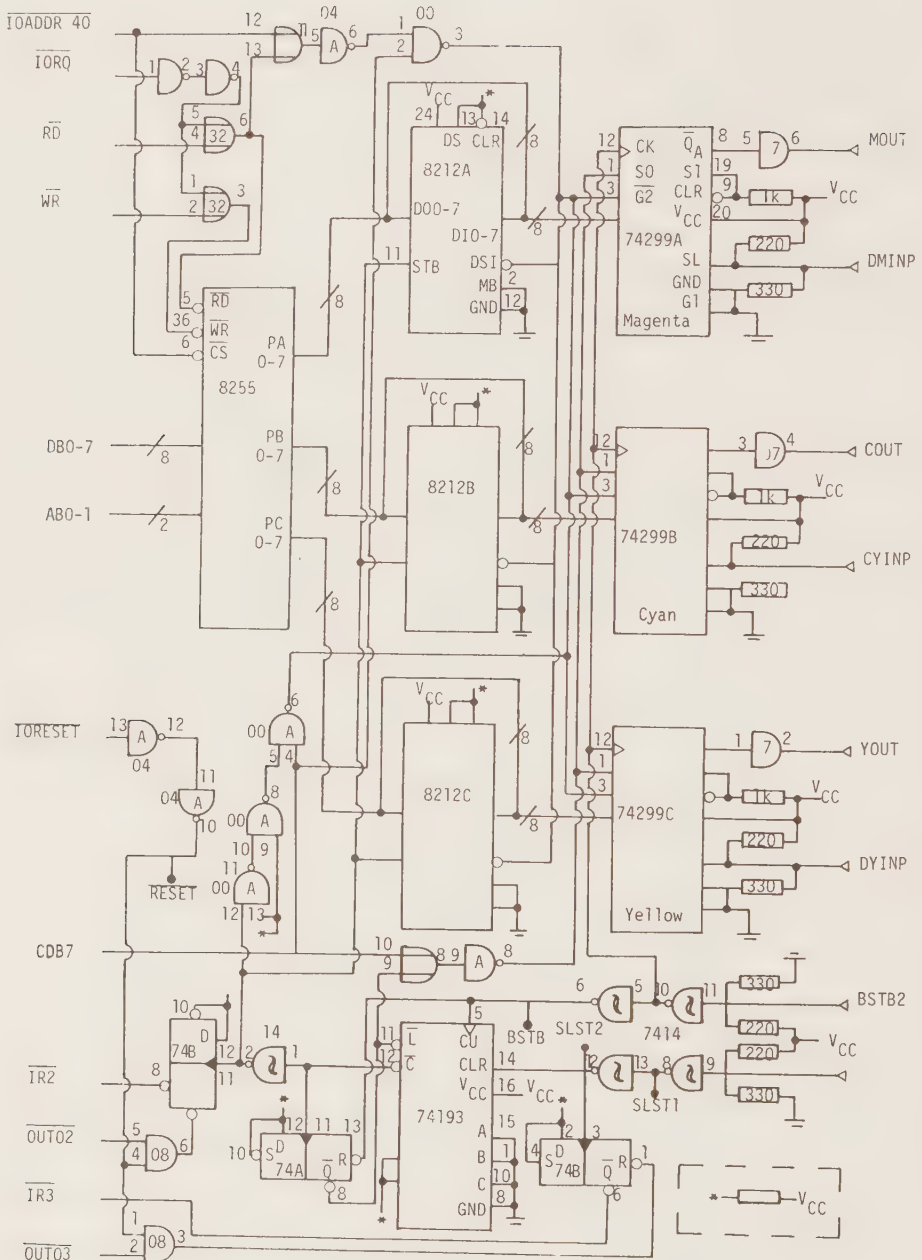


Fig A1-10 The image converter board III circuit diagram 2. This diagram includes the packing of pixels circuitry for the three colors, the microprocessor interface and the next scan line interrupt circuitry.

The communication between the scanner analog system, and between the image converter board II and III are carried out through front panel connectors. The pin configurations for the different connectors are given below.

Data direction as seen from the board	Pin number	Signal mnemonics	Short translation
input	1	MINP	Magenta INPut
"	2	CINP	Cyan INPut
"	3	YINP	Yellow INPut
"	4	BSTB2A	BitSTroBe 0.2 mm
"	5	SLSTBA	Scan Line STroBe
output	6	STEP	STEPper motor pulse
"	7	DIR	stepper motor DIREction
input	8	HOMES	HOME indicator Set
"	9	ENDS	END indicator Set
output	10	MOUT	Magenta OUTput, plotting
"	11	COUT	Cyan OUTput, plotting
"	12	YOUT	Yellow OUTput, plotting
"	13	DRCNTRL	DRum motor CoNTRoL
"	14	SLCNTRL	Scanner Light CoNTRoL
	15-20		Not used
input	21	HOMER	HOME indicator, reset
"	22	ENDR	END indicator, reset
	23-24		Not used
	25	GND	GrouND

Table A1-1 Pin assignment in female 25 pole Cannon connector to/from analog system. The connector is mounted in the shared front panel of the image converter boards I and II.

Data direction as seen from the board	Pin number	Signal mnemonics	Short translation
output	1	DMINP	Digital Magenta INPut
"	2	CINP	Digital Cyan INPut
"	3	YINP	Digital Yellow INPut
"	4	BSTB2	BitSTroBe 0.2 mm
"	5	SLSTB	Scan Line STroBe
input	6	STEP	STEPper motor pulse
"	7	DIR	stepper motor DIRection
output	8	DHOME	HOME indicator Set
"	9	DEND	END indicator Set
input	10	MOUT	Magenta OUTput, plotting
"	11	COUT	Cyan OUTput, plotting
"	12	YOUT	Yellow OUTput, plotting
	13-14		Not used
	15	GND	Ground

Table A1-2 Pin assignment in female 15 pole Cannon connector connecting the image converter boards II and III. The connector is mounted on the shared front panel of the image converter boards I and II.

Data direction as seen from the board	Pin number	Signal mnemonics	Short translation
input	1	DMINP	Digital Magenta INPut
"	2	CINP	Digital Cyan INPut
"	3	YINP	Digital Yellow INPut
"	4	BSTB2	BitSTroBe 0.2 mm
"	5	SLSTB	Scan Line STroBe
output	6	STEP	STEPper motor pulse
"	7	DIR	stepper motor DIRection
input	8	DHOME	HOME indicator Set
"	9	DEND	END indicator Set
output	10	MOUT	Magenta OUTput, plotting
"	11	COUT	Cyan OUTput, plotting
"	12	YOUT	Yellow OUTput, plotting
	13-14		Not used
	15	GND	Ground

Table A1-3 Pin assignment in female 15 pole Cannon connector connecting the image converter boards II and III. The connector is mounted on the front panel of the image converter board III.

Frontpanel

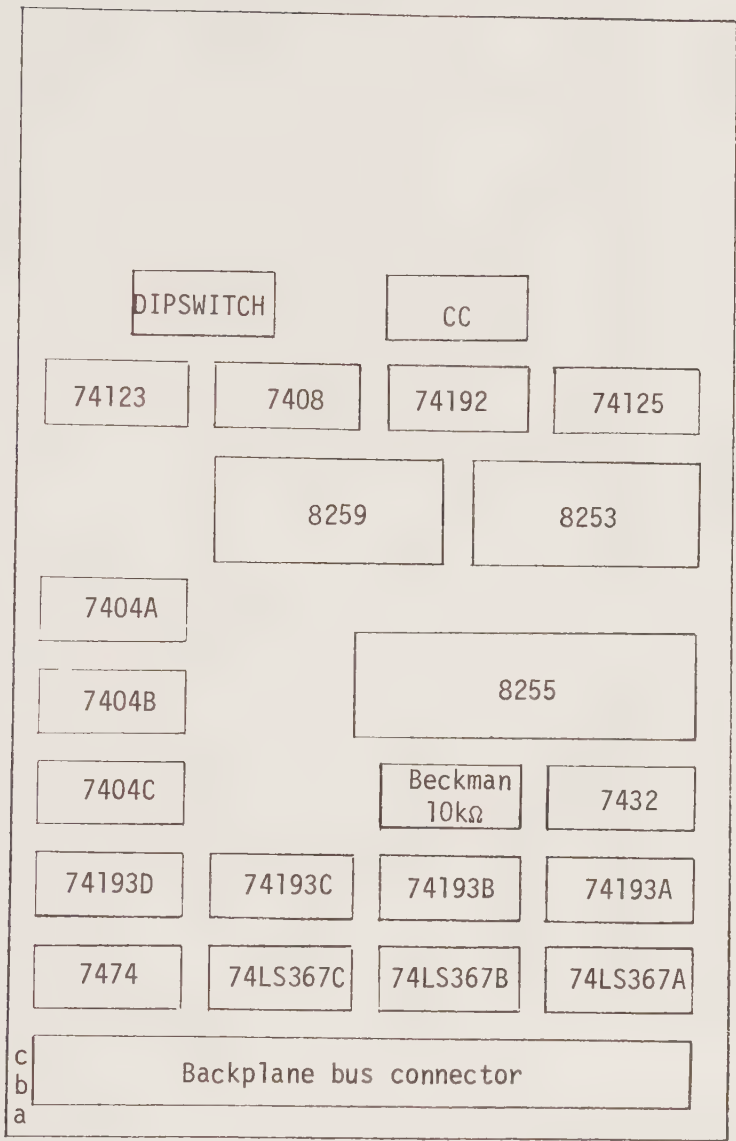


Fig A2-1 The programmable interrupt controller and DMA controller register and counter component layout. Board seen from component side.

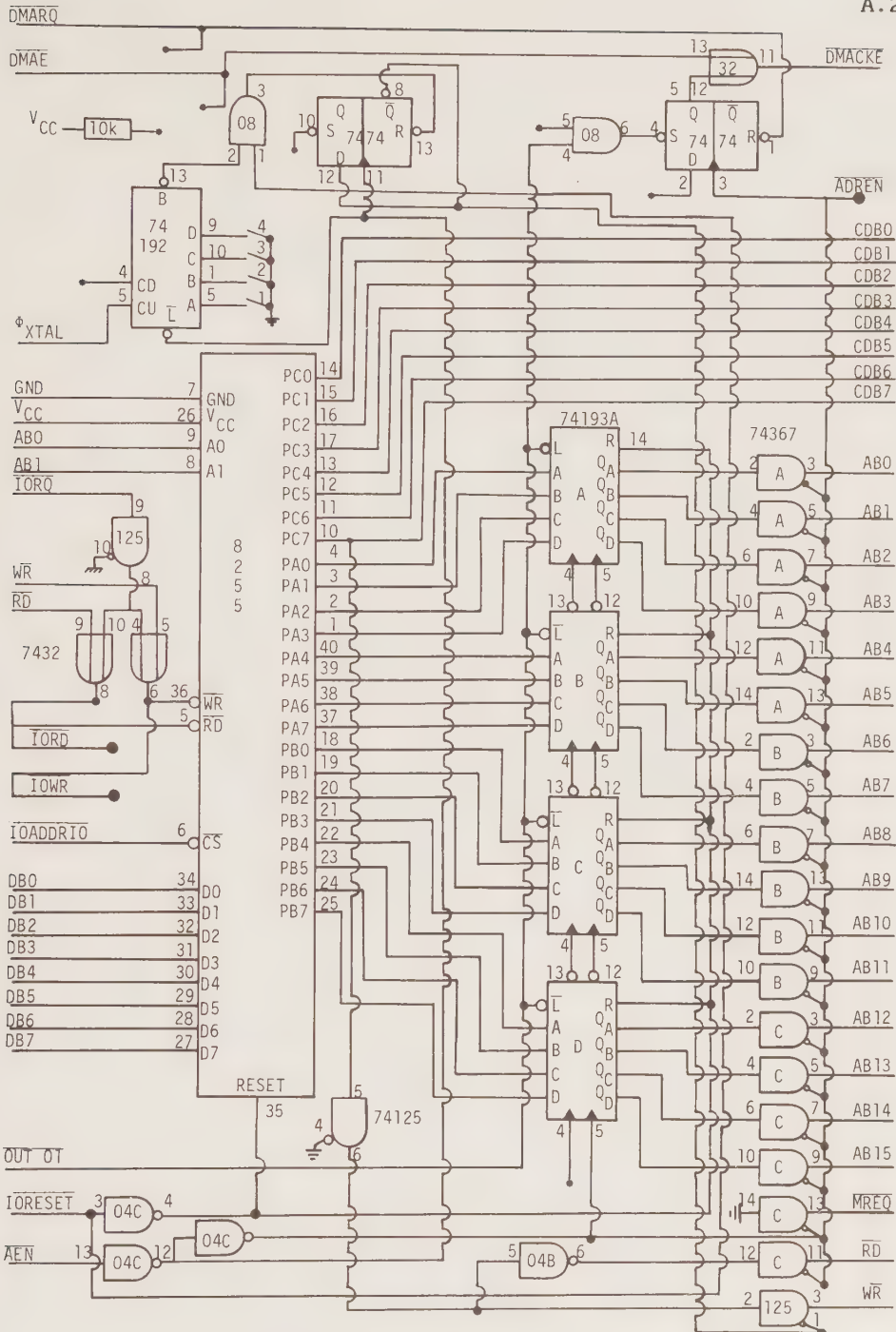


Fig A2-3 The programmable interrupt controller and DMA controller register and counter circuit diagram. This diagram includes the DMA controller start address register and address counter.

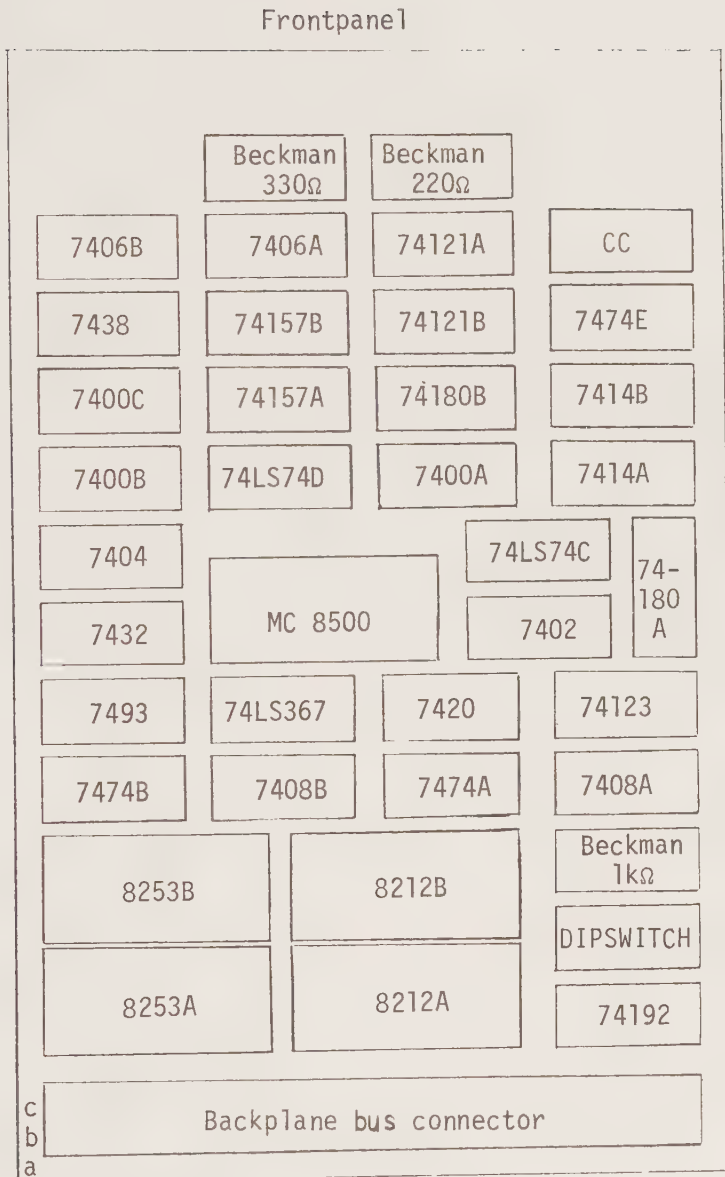


Fig A3-1 The magtape formatter board component layout. Board seen from component side.

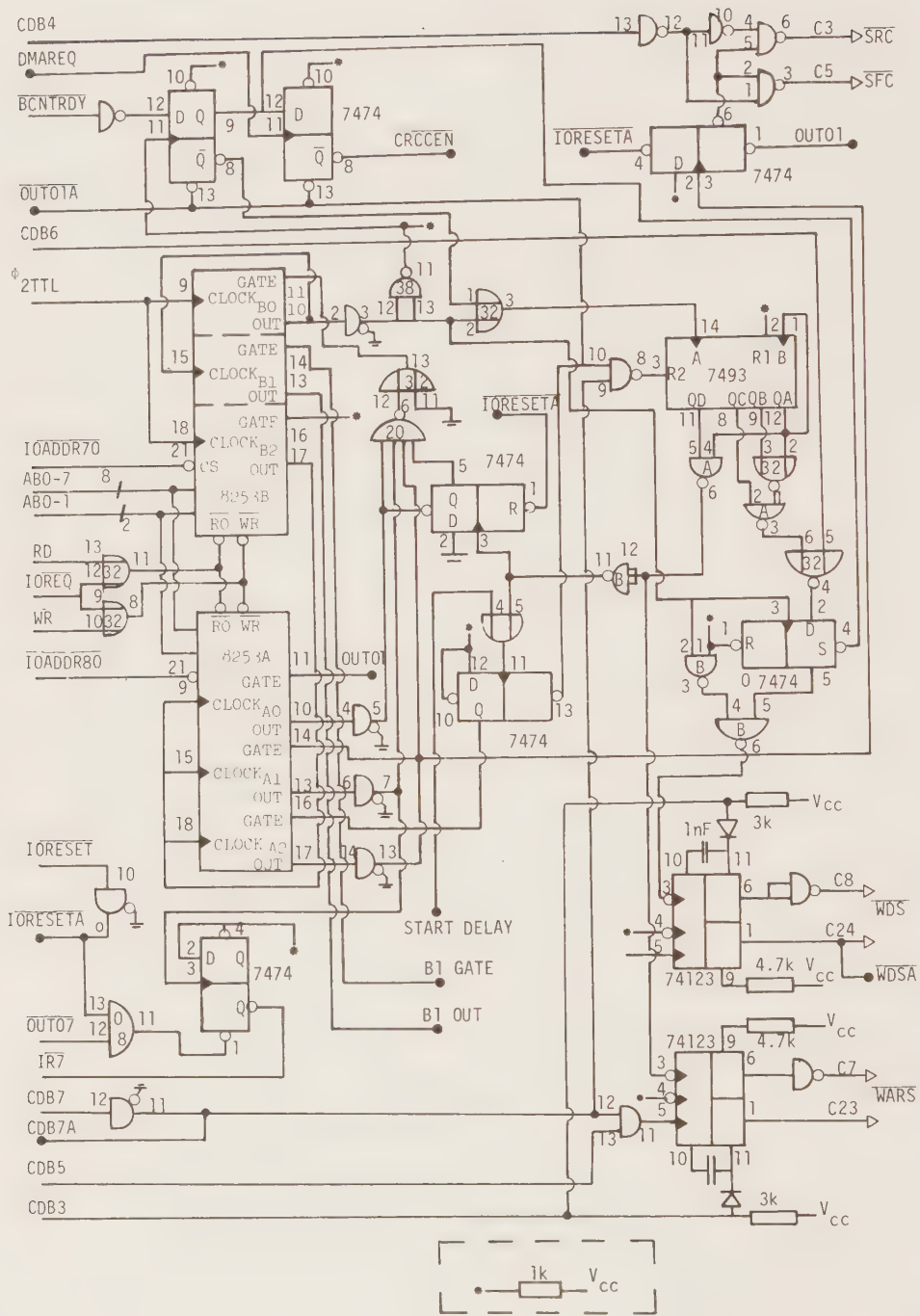


Fig A3-2 The magtape formatter board circuit diagram 1. This diagram includes the timing and control section of the magtape formatter.

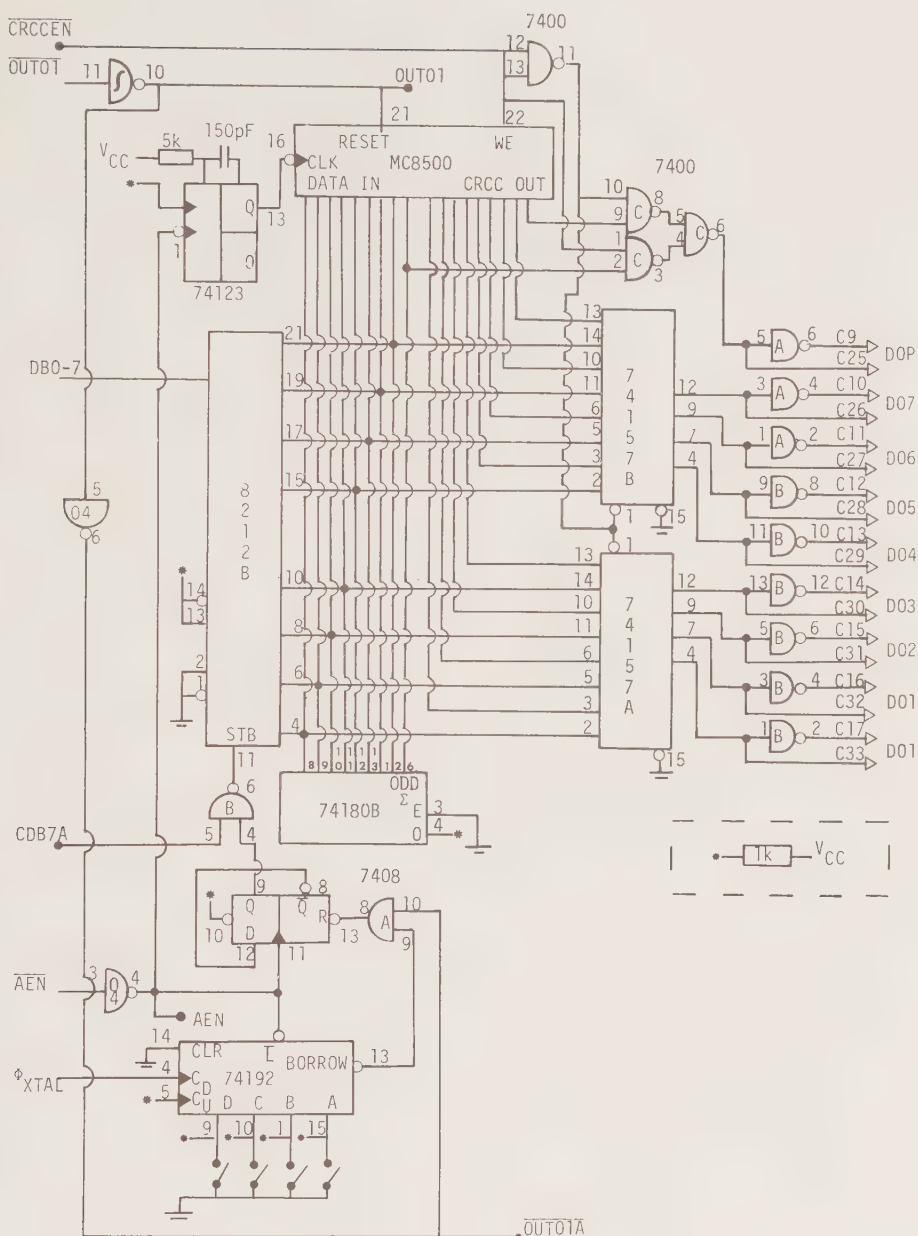


Fig A3-3 The magtape formatter board circuit diagram 2. This diagram includes the section for writing data to the tape.

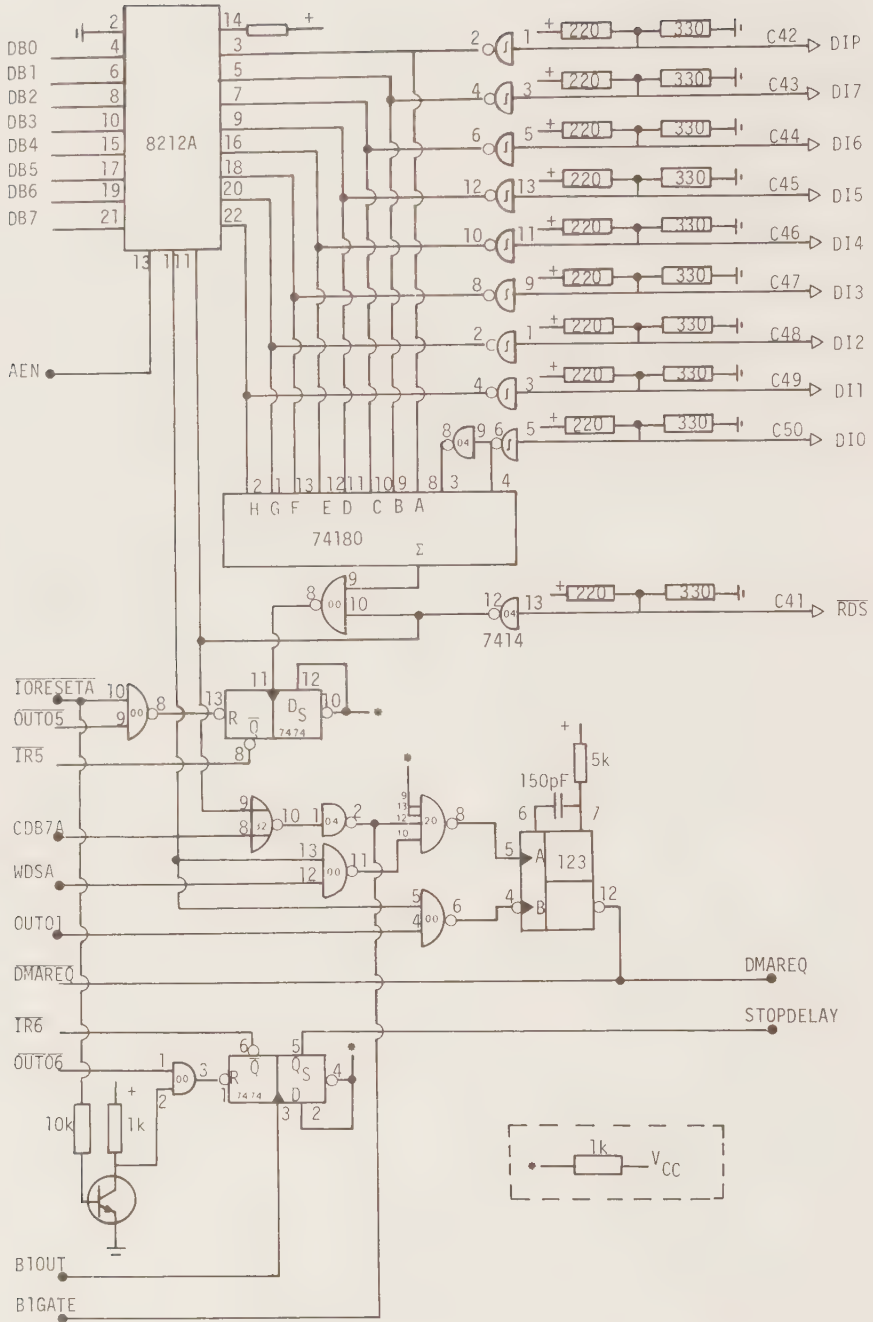


Fig A3-4 The magtape formatter board circuit diagram 3. This diagram includes the section for reading data from the tape. This section is not used in the scanner system.

Data direction as seen from the board	Pin number	Signal mnemonics	Short translation
=====			
	1	GND	GrouND
output, open collector	3	$\overline{\text{SRC}}$	Synchronous Reverse Command
"	5	$\overline{\text{SFC}}$	Synchronous Forward Command
"	6	$\overline{\text{RTH}}$	Read ThresHold
"	7	$\overline{\text{WARS}}$	Write Amplifier Reset Strobe
"	8	$\overline{\text{WDS}}$	Write Data Strobe
"	9	$\overline{\text{DOP}}$	Data output, Parity bit
"	10	$\overline{\text{DO7}}$	" , Bit 7
"	11	$\overline{\text{DO6}}$	" , " 6
"	12	$\overline{\text{DO5}}$	" , " 5
"	13	$\overline{\text{DO4}}$	" , " 4
"	14	$\overline{\text{DO3}}$	" , " 3
"	15	$\overline{\text{DO2}}$	" , " 2
"	16	$\overline{\text{DO1}}$	" , " 1
"	17	$\overline{\text{DO0}}$	" , " 0
"	18	GND	GrouND
output, TTL	23	$\overline{\text{WARS}}$	Write Amplifier Reset Strobe
"	24	$\overline{\text{WDS}}$	Write Data Strobe
"	25	$\overline{\text{DOP}}$	Data output, Parity bit
"	26	$\overline{\text{DO7}}$	" , Bit 7
"	27	$\overline{\text{DO6}}$	" , " 6
"	28	$\overline{\text{DO5}}$	" , " 5
"	29	$\overline{\text{DO4}}$	" , " 4
"	30	$\overline{\text{DO3}}$	" , " 3
"	31	$\overline{\text{DO2}}$	" , " 2
"	32	$\overline{\text{DO1}}$	" , " 1
"	33	$\overline{\text{DO0}}$	" , " 0
"	34	GND	GrouND
input	41	$\overline{\text{RDS}}$	Read Data Strobe
"	42	$\overline{\text{DIP}}$	Data input, Parity bit
"	43	$\overline{\text{DI7}}$	" , Bit 7
"	44	$\overline{\text{DI6}}$	" , " 6
"	45	$\overline{\text{DI5}}$	" , " 5
"	46	$\overline{\text{DI4}}$	" , " 4
"	47	$\overline{\text{DI3}}$	" , " 3
"	48	$\overline{\text{DI2}}$	" , " 2
"	49	$\overline{\text{DI1}}$	" , " 1
"	50	$\overline{\text{DI0}}$	" , " 0

Table A3-1 Pin assignment in female 50 pole Cannon connector to/from magtape station. Through this connector the image information is transferred to the magtape station.

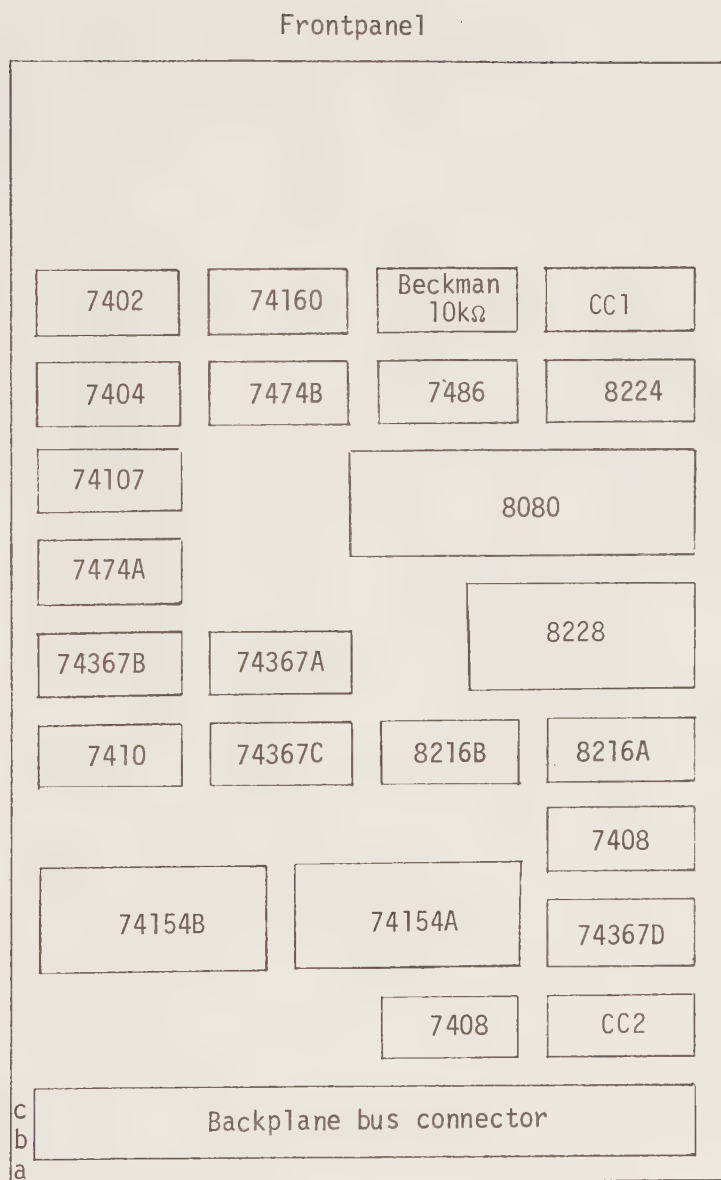


Fig A4-1 The microprocessor board component layout. Board seen from component side.

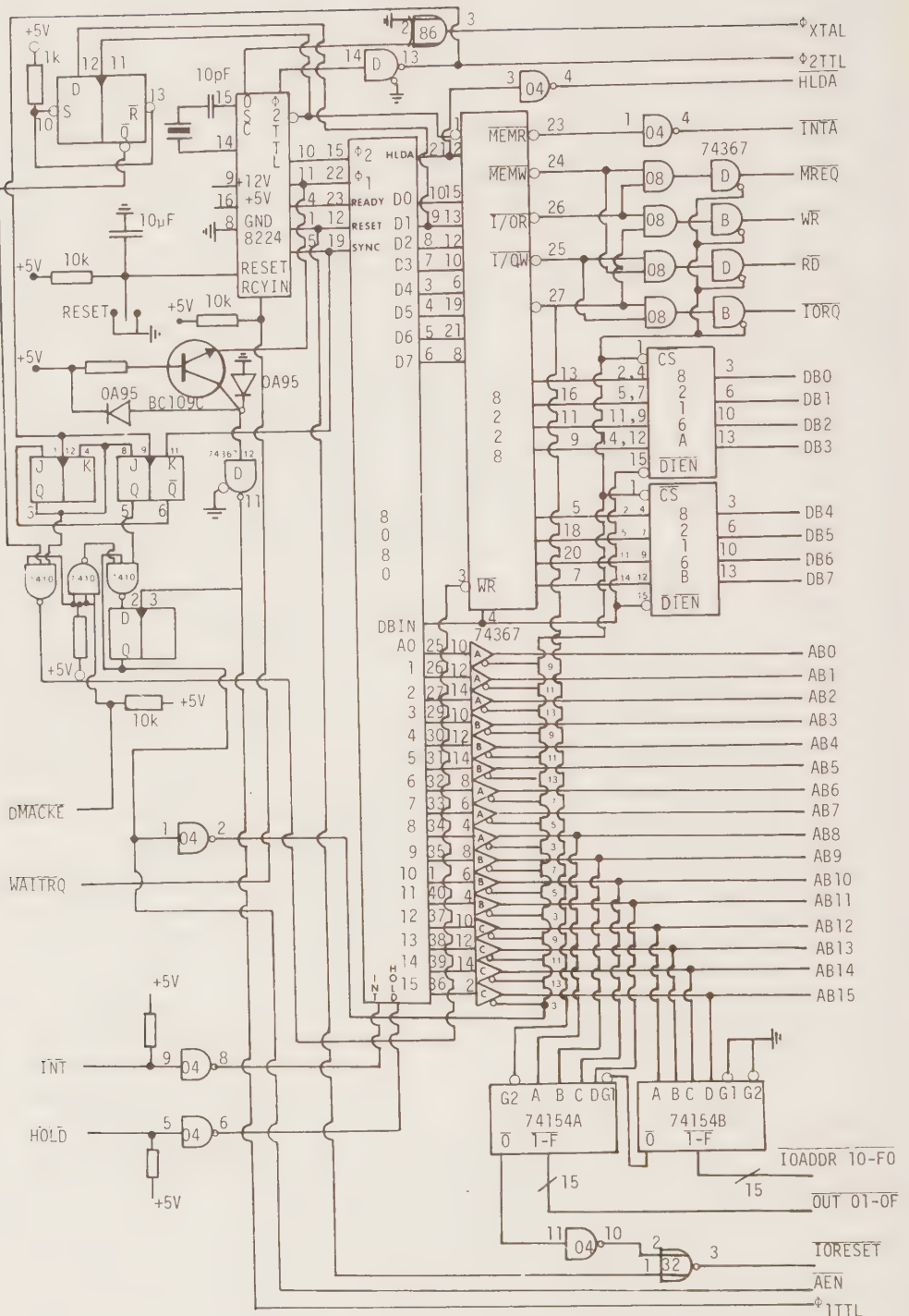


Fig A4-2 The microprocessor board circuit diagram. This diagram includes the microprocessor, the CMOS to TTL converter, the address predecoder, the sixteen 1 bit output ports and the DMA controller logic.

APPENDIX B

Microprocessor system I/O addresses in the scanner system.

Port/register
address in
hexadecimal
notation

mnemonics

function

00	<u>IORESET</u>	Reset signal for all I/O devices
01	<u>DMASTART</u>	Start signal for DMA transfers
02	<u>OUTO2</u>	Reset of IR2 interrupt D flipflop
03	<u>OUTO3</u>	" IR3 "
04	<u>OUTO4</u>	" IR4 "
05	<u>OUTO5</u>	" IR5 "
06	<u>OUTO6</u>	" IR6 "
07	<u>OUTO7</u>	" IR7 "
08	<u>ENDRESET</u>	" IR1 "
09	<u>HOMERESET</u>	" IR1 "
0D	<u>FSTEP</u>	Forced start of stepper motor
10	<u>DMASLOW</u>	DMA start address low byte port
11	<u>DMASHIGH</u>	" high byte port
12	<u>CDB</u>	Control data bus port
13	<u>DMACNTRL</u>	Control register for ports 10-12
20	<u>DMABYTECNT</u>	Bytes to transfer counter
21	<u>DMAINDICATOR</u>	DMA indicator on front panel counter
22	<u>RTC</u>	Real time clock counter
23	<u>CNTACNTRL</u>	Control register for counters 20-22
30	<u>INTCO</u>	Programmable interrupt controller low port
31	<u>INTC1</u>	" high port
40	<u>SCANMAGENTA</u>	Scanner/Plotter input/output port, magenta
41	<u>SCANCYAN</u>	" , cyan
42	<u>SCANYELLOW</u>	" , yellow
43	<u>SCANCNTRL</u>	Control register for ports 40-42
50	<u>STEP</u>	Stepper motor controller counter
51	Not used	
52	Not used	
53	<u>STEPCNTRL</u>	Control register for counters 50-52
60	<u>MAGAPORT</u>	Magtape control output port
61	<u>MAGBPORT</u>	Magtape status input port
62	<u>MAGCPORT</u>	Magtape control/status output/input port
63	<u>MAGCNTRL</u>	Control register for ports 60-62

64	GPA	General purpose port unbuffered
65	GPB	"
66	GPC	"
67	GPCNTRL	Control register for ports 64-66
70	DATARATE	Data rate to tape counter
71	GAPDETECT	Missing RDS pulses counter
72	PRESCALER	Prescaler counter on formatter board
73	COUNTCNTRL	Control register for counters 70-72
80	MSTART	Magtape start delay counter
81	MRAMP	Magtape stop delay counter
82	MSTOP	Magtape stop write delay counter
83	DELAYCNTRL	Control registers for counters 80-82
A0	DITMAGENTA	Dither matrix RWM address and magenta threshold data
A1	DITCYAN	Dither matrix cyan threshold data
A2	DITYELLOW	" yellow threshold data
A3	DITCNTRL	Control register for ports A0-A2
A4	DRUMON	Enable drum rotation
A5	DRUMOFF	Disable drum rotation
A6	ONLIGHT	Scanner light ON
A7	OFFLIGHT	" OFF
A8	DRLC	Normal scanning operation
A9	<u>DRLC</u>	Dither threshold RWM load enable
AA	DRAL	Dither threshold RWM data load enable
AB	<u>DRAL</u>	Dither threshold RWM address load enable
AC	DRR/W	Dither threshold RWM read enable
AD	<u>DRR/W</u>	Dither threshold RWM write enable
AE	DRDC	Dither threshold RWM output disable
AF	<u>DRDC</u>	Dither threshold RWM output enable
F4	QTYDATA	USART data port to/from host computer
F5	QTYCNTRL	USART control register
FA	TTYDATA	USART data port to/from operator terminal
FB	TTYCNTRL	USART control register

APPENDIX C

Backplane bus and front panel connector mnemonics in alphabetical order.

ABO-15	16 bit address bus
AEN	DMA Address ENable, c.f. chapter 4.2.5
BCNTRDY	Byte CouNT ReaDY, c.f. chapter 4.2.5
BSTB1	Bitstrobe signal originating from shaft encoder, c.f. chapter 4.2.2
BSTB2	Bitstrobe signal originating from shaft encoder, c.f. chapter 4.2.2
BSTB2A	Bitstrobe signal originating from shaft encoder, c.f. chapter 4.2.2
CDBO-7	Control data bus, c.f. chapter 4.3.8.2
CINP	Cyan INPut signal, c.f. appendix A1
COUT	Cyan OUTput signal not used in the scanner system
DBO-7	8 bit data bus
DDS	Data Density Select in magtape station, c.f. chapter 4.2.7
DEND	END position signal, c.f. chapter 4.2.8.3
DHOME	HOME position signal, c.f. chapter 4.2.8.3
DIO-7,DIP	Data inputs from magtape station, not used in the scanner system
DIR	Stepper DIRection of stepper motor, c.f. chapter 4.2.8.5
DMACKE	DMA ClocK Enable, c.f. chapter 4.2.5 and appendix A2
DMAE	DMA Enable, c.f. chapter 4.2.8.5
DMAREQ	DMA REQuest, c.f. chapter 4.2.8.5
DOO-7,DOP	Data outputs to magtape station, c.f. tableA3-5
DRAL	Dither RWM Address Load enable/disable, c.f. chapter 4.2.1
DRCNTRL	DRum motor CoNTRoL, c.f. chapter 4.2.1
DRDC	Dither RWM Data Check enable/disable, c.f. chapter 4.2.1
DRLC	Dither RWM Load Cycle enable/disable, c.f. chapter 4.2.1
DRR/W	Dither RWM Read/Write, c.f. chapter 4.2.1

END	End position signal for scanner head, c.f. chapter 4.2.8.3
ENDR	End position signal for scanner head, c.f. chapter 4.2.8.3
ENDS	End position signal for scanner head, c.f. chapter 4.2.8.3
EOT	End Of Tape, status signal from magtape station, c.f. chapter 4.2.7
FPT	File write ProTect, status signal from magtape station, c.f. chapter 4.2.7
GAPDETECT	Inter record GAP DETECT during tape read operation, signal not used in the scanner system
HDI	High DensITy, status signal from magtape station, c.f. chapter 4.2.7
HLDA	HoLD Acknowledge, signal on back plane bus not used in the scanner system
HOLD	Microprocessor HOLD, signal on back plane bus not used in the scanner system
HOME	Home position signal for scanner head, c.f. chapter 4.2.8.3
HOMER	Home position signal for scanner head, c.f. chapter 4.2.8.3
HOMES	Home position signal for scanner head, c.f. chapter 4.2.8.3
INT	INTerrupt request signal from the PIC to the microprocessor
INTA	INTerrupt request Acknowledge from the microprocessor to the PIC
IOADDR10-FO	Predecoded IOADDRESS, c.f. chapter 4.2.8.1
IORESET	IORESET signal, c.f. chapter 4.2.8.1
IOREQ	I/O REQuest signal used when addressing an I/O device, as opposed to the MREQ signal used when addressing a memory cell
IRO-7	8 Interrupt Request signals , c.f. chapter 3.4.1 and 4.2.1
LDP	At LoaD Point, status signal from the magtape station, c.f. chapter 4.2.7
LOL	Load On Line, control signal to the magtape station, c.f. chapter 4.2.7

MINP	Magenta INPut digital signal, c.f. appendix A1
MOUT	Magenta OUTPut digital signal used for plotting, not used in the scanner system
MREQ	Memory REQuest signal used when addressing a memory cell, as opposed to the IOREQ signal used when addressing an I/O device
OFFC	OFFline Command, control signal to the magtape station, c.f. chapter 4.2.7
ONL	ONLine, status signal from magtape station, c.f. chapter 4.2.7
OUT00	I/O reset signal, c.f. chapter 4.2.8.1
OUT01	Start new block of DMA transfers signal, c.f. chapter 4.2.5 and 4.2.8.1
OUT02-09	Reset signals for interrupt requests IRL-7, c.f. chapter 4.2.3 and 4.2.8.1
OUTOD	Force stepper motor step enable, c.f. 4.2.8.5
OVW	OverWrite, control signal to the magtape station, c.f. chapter 4.2.7
RD	ReaD signal, reading from memory or I/O depending on the status on the MREQ and IOREQ signals.
RDS	Read Data Strobe signal from magtape station, not used in the scanner system
RDY	Magtape station ReaDY, status signal from the magtape station, c.f. chapter 4.2.7
RNG	Tape RunniNG, status signal from the magtape station, c.f. chapter 4.2.7
RTH	Read ThresHold, control signal to the magtape station, c.f. chapter 4.2.7
RWC	ReWind Command, control signal to the magtape station, c.f. chapter 4.2.7
RWD	ReWinDing, status signal from the magtape station, c.f. chapter 4.2.7
SFC	Synchronous Forward Command, control signal to the magtape station, c.f. chapter 4.2.7
SLCNTRL	Scanner Light CoNTRol signal, c.f. chapter 4.2.8.4
SLSTB	Scan Line STroBe signal, c.f. chapter 2.5 and appendix A1
SLSTBA	Scan line strobe signal, c.f. chapter 2.5 and appendix A1
SLT0-2	SeLecT magtape unit address lines, control signals to the magtape station, c.f. chapter 4.2.7

SRC	Synchronous Reverse Command, control signal to the magtape station, c.f. chapter 4.2.7
STEP	STEPping pulses to the stepper motor, c.f. chapter 4.2.8.4
SWS	Set Write Status, control signal to the magtape station, c.f. chapter 4.2.7
WAITRQ	WAIT ReQuest signal present in back plane bus, not used in the scanner system
WARS	Write Amplifiers Reset Strobe, control signal to the magtape station, c.f. chapter 4.2.7
WDS	Write Data Strobe, control signal to the magtape station, c.f. chapter 4.2.7
WEN	Write ENable, control signal to the magtape station, c.f. chapter 4.2.7
WR	WRite signal, writing to memory or I/O depending on the status of the MREQ and IOREQ signals. The microprocessors own WR signal is not used, c.f. chapter 4.2.5
YINP	Yellow INPut digital signal, c.f. appendix A1
YOUT	Yellow OUTput digital signal for plotting, not used in the scanner system

